A Power Supply Topology Operating at Highly Discontinuous Input Voltages for Two-Wire Connected Control Devices in Digital Load-Side Transmission (DLT) Systems for Intelligent Lighting

Lukas Lohaus, Arne Rossius, Ralf Wunderlich and Stefan Heinen

Integrated Analog Circuits and RF Systems Laboratory,
RWTH Aachen University,
Sommerfeldstrasse 24, 52074 Aachen, Germany
Email: ias@rwth-aachen.de.

***Abstract*—This paper presents a power supply concept for control devices in Digital Load-Side Transmission (DLT) systems delivering a high energy output. The proposed topology consists of two stages, a boost converter and a flyback converter. As a direct replacement for conventional light switches or dimmers, this power supply works without a neutral wire connection and is supplied with energy compliant to the DLT specification [1] through a switched bypass structure in the series connected DLT luminaire. This method enables the application of DLT systems in existing installations, which typically lack a neutral wire at the light switch lead-out. Although operating at a highly discontinuous and varying input voltage, the proposed two-stage topology provides a continuous high output power of maximum $P_{out,max} = 475\,\mathrm{mW}$. Input voltages of up to $100\,\mathrm{V}$ can be handled. The output voltage is regulated to $3.3\,\mathrm{V}$, a typical value to supply microcontrollers with attached periphery, e.g. common WiFi modules [2], [3]. It is shown that the measured output power is high enough to operate a WiFi frontend. Completely new functionality, such as integrating a DLT control device into a smart home infrastructure, is hence realized.**

I. Introduction

As lighting loads are estimated to make up about $19\,\%$ of the world-wide power consumption [4], the introduction of high efficiency light sources, such as light emitting diodes (LEDs), offers great potential in terms of cutting the overall energy usage down. In consequence, many suitable LED driving systems with high energy efficiency have been developed [5]–[7]. In combination with applying intelligent features, like presence detection or automatic light intensity adaption, it is expected to achieve even higher energy savings [8]. Hence, wireless and wirebound communication systems have been applied to LED drivers in order to embed LED luminaires in a smart home environment. Suitable implementations are provided in literature for both methodologies [9]–[14].

Recently, the power line communication methodology 'Digital Load-Side Transmission' (DLT) has been evolved for intelligent lighting solutions in homes and small offices and is about to be standardized [1], [15]. DLT fulfills the demands of a modern lighting system by providing full color control, color temperature adaption and dimming functionality and thus represents a robust, low cost alternative to ZigBee or Bluetooth controlled lighting systems. In fact, DLT control devices are meant to replace conventional light switches or dimmers and are hence directly operated from the utility grid. Unfortunately, the wiring in old houses does often not provide a neutral wire at the light switch lead-out, but only features the phase wire. Therefore, DLT copes with this restriction and uses a series connection with the luminaire like the existing light switch for compatibility reasons. However, this puts strong limitations on the power supply of a control device, which is explained in detail in the subsequent section.

The overall aim of this research is to integrate a DLT subsystem into a smart home environment by using a wireless uplink. Therefore, this paper presents a power supply concept that conforms to the DLT specifications and delivers enough output power for operating a WiFi module in addition to the required control device circuitry. Because the power consumption of a WiFi module is higher than that of a Bluetooth or ZigBee one, the same power supply unit can also be used for those communication methods without change. Of course, outstanding AC-DC converter solutions coping with a sinusoidal AC utility grid input voltage of $230\,\mathrm{V_{RMS}}$ and delivering a constant DC output voltage of e.g. $3.3\,\mathrm{V}$ for peripheral devices exist [16]–[19]. Though, these converter solutions are not applicable because they cannot be operated, if no neutral wire is present at the dimmer lead-out. To the best of the authors' knowledge no DLT control device exists that provides enough energy for powering a WiFi module and in consequence connect a DLT control device to an intelligent backbone infrastructure via this gateway. To overcome this issue, this paper presents a power supply topology that can handle the highly discontinuous input voltage conditions while providing high output power at a constant DC output voltage.

The presented paper is divided into five different sections. After a short introduction to DLT and smart lighting environments in the first section, section II explains the requirements and boundary conditions of the DLT system in detail with respect to operating a relatively high-power consuming load like a WiFi module. Subsequently, section III proposes the AC-DC power supply concept that complies with the DLT standard.

978-1-4799-6735-3/15/$31.00

In section IV measurement data on achieved output power and efficiency are provided. Finally, section V summarizes the gained achievements and concludes this work.

II. Boundary Conditions for DLT systems and Power Supply System Requirements

This section highlights two aspects of the system requirements for an efficient DLT compatible power supply topology.

A. The limiting boundary conditions required by the DLT specifications [1]

B. The additional power demand caused by a common WiFi module and other periphery

In the following, all computations are performed under the assumption of the European utility grid with a grid frequency of $f_{grid} = 50\,\text{Hz}$ and a root-mean-sqaure (RMS) grid voltage of $V_{grid,RMS} = 230\,\text{V}$.

A. Boundary Conditions for DLT control devices

As mentioned above, DLT has been developed as a replacement technology for conventional lighting installations. Hence, it works without a neutral wire connection at the light switch lead-out. In fact, a DLT control device may only power itself in a defined supply period shortly after every zero crossing of mains voltage, which requires a suitable bypass structure in the series-connected luminaire. The supply period ends when mains voltage exceeds V_{SW} as defined by the DLT specification [1]. It can further be subdivided into two low current (LC) phases and one high-current (HC) phase. In terms of available supply energy the LC intervals can be neglected and only the HC phase is considered. Fig. 1 illustrates the specified DLT supply period with the respective LC and HC intervals and maximum possible current draw. The DLT specification allows for a voltage drop across the series-connected luminaire of up to 20 V during the HC interval. The resulting ideal (no drop, solid line) as well as worst-case (full 20 V drop, dashed line) voltages across the control device (CD) are also depicted in Fig. 1.

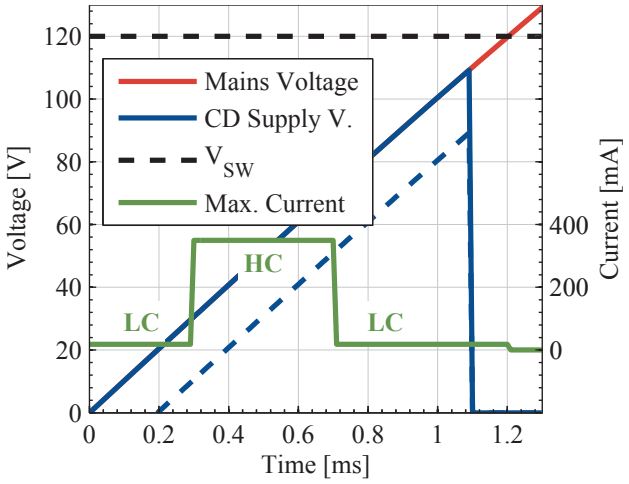


Fig. 1. DLT supply period with maximum available input current [1].

As can be seen from the graph, the HC phase starts at $t_1 = 300\,\mu\text{s}$ and ends at $t_2 = 700\,\mu\text{s}$ after the zero crossing of mains voltage. A control device conforming to the DLT specifications [1] may not draw a higher input current than $I_{CD,max} = 350\,\text{mA}$ during this time. Considering these boundary conditions of operation the maximum theoretically available energy per halfwave can be calculated as follows.

$$W_{CD,max} = \int_{t_1}^{t_2} \hat{V}_{grid} \cdot \sin(2\pi f_{grid} t) \cdot I_{CD,max}\, dt \tag{1}$$
$$= \int_{300\,\mu\text{s}}^{700\,\mu\text{s}} \sqrt{2} \cdot 230\,\text{V} \cdot \sin(2\pi \cdot 50\,\text{Hz} \cdot t) \cdot 350\,\text{mA}\, dt$$
$$= 7.12\,\text{mJ}$$

Accordingly, the minimum available energy per halfwave, if a voltage drop of $V_{drop} = 20\,\text{V}$ across the luminaire occurs, can be determined by equation 2

$$W_{CD,min} = \int_{t_1}^{t_2} (\hat{V}_{grid} \cdot \sin(2\pi f_{grid} t) - V_{drop}) \cdot I_{CD,max}\, dt \tag{2}$$
$$= 4.32\,\text{mJ}$$

These values correspond to an average output power of $P_{CD,max} = 712\,\text{mW}$ and $P_{CD,min} = 432\,\text{mW}$, respectively.

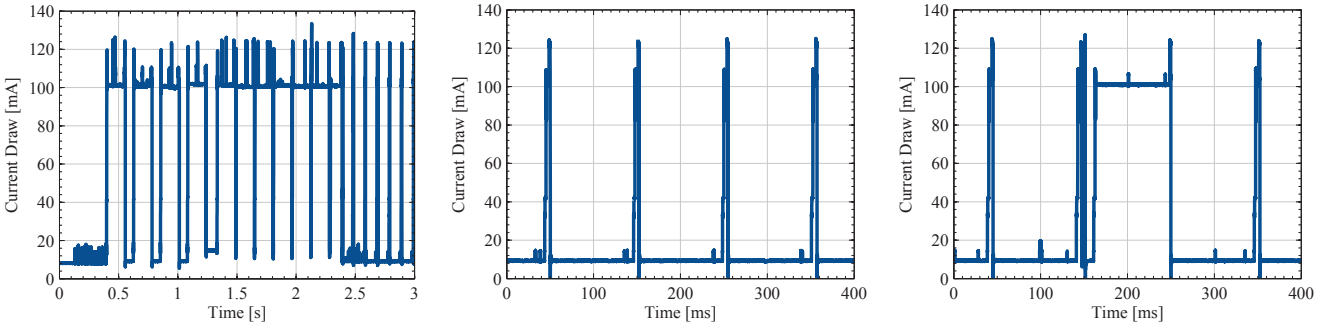
B. Expected power demand of periphery

In order to check whether the available power can fulfill the demands of a power-hungry WiFi module and additional periphery, such as a liquid crystal display (LCD), measurements on the current consumption of a common WiFi module [2] have been taken in different modes of operation while a constant DC supply voltage has been applied. Fig. 2a to Fig. 2c illustrate the corresponding results. It can be seen that the WiFi module never exceeds an average current draw of around 110 mA in all cases. For the presented implementation the so-called power-save mode should be used as depicted in Fig. 2b. In this mode of operation the WiFi frontend only wakes up every 100 ms, hence reducing overall power consumption. In case of data transfer within this power-save mode, the WiFi module requires a transmit and receive time of about 100 ms for low data volume as shown in Fig. 2c.

The worst case scenario is indeed the power consumption of the association mode that occurs when a connection to an access point is established. Typically, the association phase happens only once after power-up. Fig. 2a shows the recorded measurement data for this case. For the calculation continuous current draw of $I_{WLAN,assoc} = 110\,\text{mA}$ is assumed. Hence, the worst-case power consumption $P_{WLAN,max}$ at a supply voltage of $V_{out} = 3.3\,\text{V}$ can be computed by equation 3.

$$P_{WLAN,max} = V_{out} \cdot I_{WLAN,assoc} \tag{3}$$
$$= 3.3\,\text{V} \cdot 110\,\text{mA} = 363\,\text{mW}.$$

The current consumption of the main microcontroller and additional periphery, such as an LCD, can be approximated



(a) Current draw during association phase. (b) Current draw during power-save mode. (c) Current draw during data transfer.

Fig. 2. Measurements of a common WiFi module's [2] current draw for different modes of operation at a constant 3.3 V supply voltage.

to about 10 mA. This yields an additional power consumption of

$$P_{periphery} = V_{out} \cdot I_{periphery} = 3.3\,\text{V} \cdot 10\,\text{mA} = 33\,\text{mW}. \quad (4)$$

To go without an additional power source for the WiFi association phase, it would be desirable for the proposed supply concept to provide the required output power in the described worst-case of 20 V drop across the luminaire. This would require a minimum power supply efficiency of

$$\eta_{min} = \frac{P_{WLAN,max} + P_{periphery}}{P_{CD,min}} = 92\,\%. \quad (5)$$

In fact, this aim is impractical to achieve with a two-stage power supply concept. However, if a reasonably well designed luminaire is used, the voltage drop is usually below 5 V. In this case the efficiency requirement drops sufficiently to make an implementation of a DLT compatible power supply feasible. In consequence, the aim of the proposed power supply concept is to exploit the maximum possible energy yield out of the limited DLT supply period.

III. System Concept of a DLT Compatible AC-DC Power Supply Topology

Fig. 3 illustrates a block diagram of the proposed power supply topology consisting of two stages, a boost converter and a flyback converter. The energy taken from the grid by the first converter stage is stored on the capacitor C_{store} in order to operate the second converter stage with a continuous DC supply voltage. Additionally, an enable switch and a current limiter are connected upstream of the converters. The enable switch is meant to protect the circuit from input voltages above 100 V, which can occur outside of the HC supply phase. The current limiter is required to limit the inrush current during the initial charging of C_{store} after power-on because the boost converter topology has no means of controlling the input current in this case. This ensures that the DLT specifications are maintained as no current higher than $I_{CD,max}$ can be drawn.

In the presented implementation two microcontrollers (μCs) are used. One is the main μC for the entire DLT control device, which takes care of precise timing and controls the enable switch. The second μC is part of the boost converter's control circuitry and provides the PWM frequency and takes care of the overvoltage protection in the boost converter stage. It is inevitable to use two dedicated μCs since both tasks are timing critical. It should be noted that a small start-up circuit is necessary to start the operation of these μCs. In consequence, the enable switch remains disabled during this start-up phase. After the start-up has finished, the power supply, which has been fully realized with commercially available components, can supply itself.

In order to achieve the maximum possible energy yield out of the limited DLT supply period as calculated in equation 1, it is necessary to draw the maximum possible current and follow mains voltage as closely as possible. However, a voltage jump at the input of the power supply must not result in excessive input current. A boost converter has thus been chosen

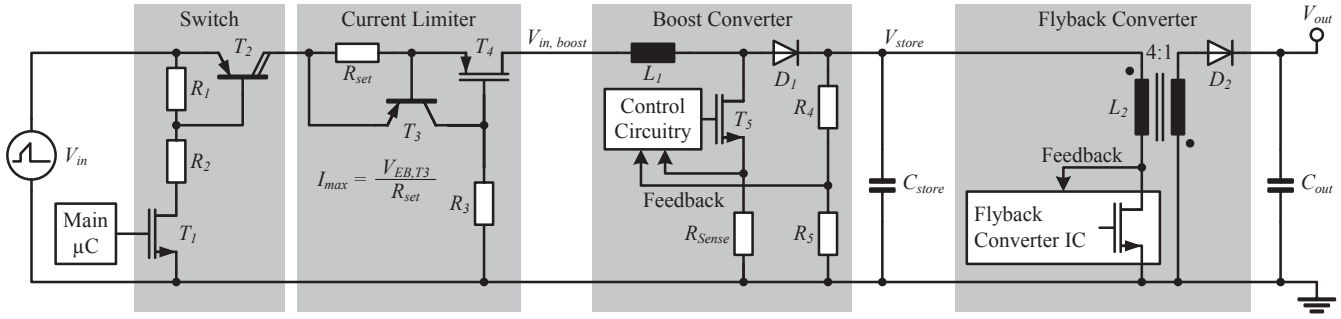


Fig. 3. System concept and circuit topology of the proposed power supply for DLT control devices

as the first stage of the power supply for the two following reasons. First, the voltage across the inductance L_1 may rise abruptly at the turn-on time t_1 while the input current ramps up from zero. Second, the inductor L_1 ensures a continuous input current flow, which is regulated by the boost converter control circuitry. Both features ensure the following of mains voltage and a continuous current draw close to the specified DLT limit at the same time. Therefore, an optimum energy yield can be achieved depending on both the dimensioning of L_1 and the converter efficiency.

Fig. 4 shows the influence of the inductor size on the input current of the boost converter. Because the maximum current limit of $I_{CD,max} = 350\,\text{mA}$ defined by the DLT standard must not be exceeded, the input current ripple determines the maximum available energy. It is shown that a lower current ripple yields a higher average input current as it is possible to move closer to the DLT limit.

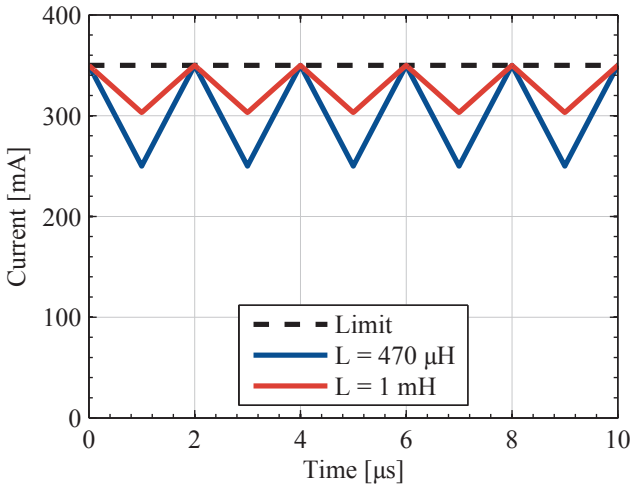


Fig. 4. Effects of inductor size on the input current of the boost converter.

As can be seen from Fig. 4, the dimensioning of L_1 is hence critical. A higher inductance value obviously yields a lower current ripple, hence increasing the possible average current draw. However, a higher inductance goes along with a bigger footprint, a longer ramp-up time at turn-on and higher ohmic losses due to a bigger parasitic resistance. The current ripple can also be decreased by selecting a higher switching frequency $f_{sw,boost}$, which on the other hand increases the dynamic losses of the converter. Therefore, the trade-off between inductor size, switching frequency and the amount of available energy needs be to be optimized.

The purpose-designed boost converter control circuitry is depicted in Fig. 5. It allows for switching frequencies of up to 1 MHz, while an inductor size of $L_1 = 1\,\text{mH}$ has been chosen for the presented implementation. The converter control uses a very simple pulse-width modulation (PWM) control methodology implemented with a discrete flip-flop. The input current is measured with a sense resistor R_{sense} and whenever it reaches the limit of $I_{CD,max} = 350\,\text{mA}$, the flip-flop turns transistor T_5 off. It should be noted that the value of R_{sense} has to be selected very carefully. If the current limit of the boost converter stage is higher than the activation level of the current limiter, which is determined by means of R_{set}, a large voltage drop across the limiter will occur resulting in massive losses and severely impacting the available output power. In this case, the transistor T_5 would continuously be conducting because the current sense level V_{sense} never reaches its limit $V_{I_{max}}$ and no more energy is transferred onto C_{store}. Hence, when selecting the values of R_{sense} and R_{set}, component tolerances have to be considered in order to account for a certain security margin. To avoid this deadlock situation, the circuit can be modified to limit the MOSFET's on-time as illustrated in Fig. 5. This is done by connecting the flip-flop's '*D*' input to its inverted output (gray dashed line) instead of tying it to V_{DD} (black dashed line) directly. This way, if the current limit hasn't been reached by the end of a PWM period, the MOSFET turns off for the next PWM period. In all other cases, the behavior of the two variants is identical.

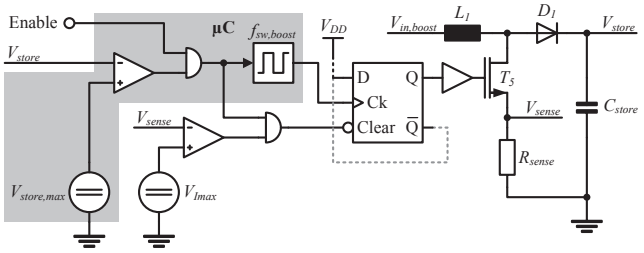


Fig. 5. Developed control circuitry of the boost converter stage.

Additionally, the converter can be switched off completely by stopping the PWM frequency $f_{sw,boost}$ and asserting the '*Clear*' input to the flip-flop. This happens in the two following cases: First, when the enable pin is pulled low, which is done by the main μC outside of the specified HC supply phase, and second, when the maximum storage voltage $V_{store,max}$ is exceeded, which occurs regularly at light load conditions.

Boosting the input voltage to a higher level enables storing of large energy portions using relatively small (ceramic) capacitors. This is because the voltage level affects the storable amount of energy quadratically, whereas the capacitance influences it only in a linear way as can be seen from equation 6.

$$W_{store} = \frac{1}{2} \cdot C_{store} \cdot V_{store}^2 \tag{6}$$

However, the storage voltage cannot be selected too high since it impairs the efficiency of the second stage and limits the number of available off-the-shelf controller integrated circuits (ICs). Therefore, C_{store} must be dimensioned accordingly. If several halfwaves of mains voltage are missing, the capacitor has to supply the second stage with energy without being recharged. To determine a reasonable value for the capacitance of C_{store} a trade-off between costs, physical size and start-up time on the one hand and available energy during blackouts on the other hand has to be considered. In the current approach, the storage capacitance is chosen to equal $C_{store} = 5\,\mu\text{F}$ and V_{store} is limited to $V_{store,max} = 91.7\,\text{V}$. By these choices the entire DLT control device can continue operation in case of up to ten successive missing mains halfwaves with the WiFi module being idle in power-save mode.

For the second stage a commercially available flyback converter IC that can handle input voltages of up to 100 V

is used [20]. This IC is optimized for applications with load currents around some hundreds of mA. In the presented implementation, the converter regulates its output to the desired 3.3 V employing a transformer L_2 with a $(4:1)$ turns ratio and a primary inductance of $L_2 = 300\,\mu\text{H}$. Generally, the flyback converter offers the opportunity to provide galvanic isolation, if needed. This is a good feature for a later target implementation in industry. However, in the realized implementation no galvanic isolation is utilized for simplicity.

Since the boost converter cannot control the input current when the voltage on C_{store} is larger than its input voltage, care must be taken to avoid this situation. For this reason, the flyback converter only turns on when the voltage on C_{store} has reached 80 V. This allows the boost converter to build up some initial charge on C_{store} before any significant power is drawn by the second converter stage.

IV. Experimental Setup and Measurement Data

Fig. 6 illustrates a photo of the implementation of the power supply concept. The board contains all of the functional blocks explained in the system concept laid out in section III.

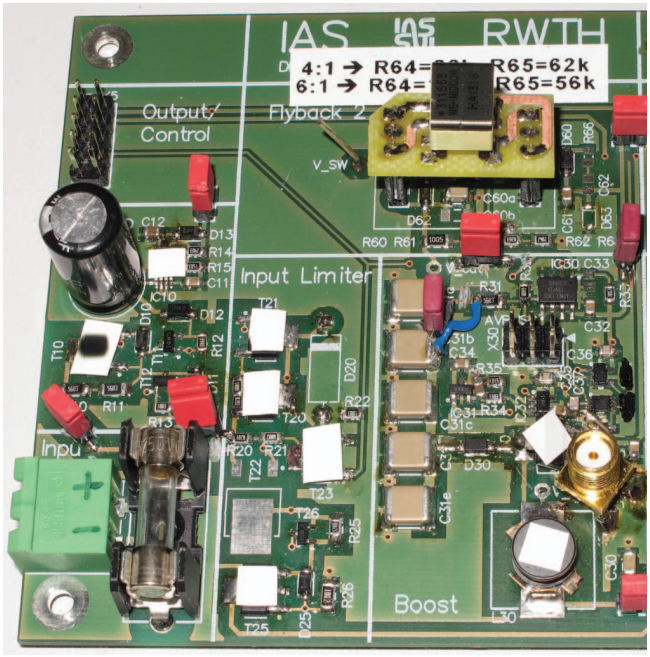


Fig. 6. Photography of the developed hardware implementation.

A measurement of input voltage and current is depicted in Fig. 7 while a constant current of $I_{load} = 125\,\text{mA}$ is drawn from the 3.3 V DC output of the flyback converter. The voltage applied to the input of the converter has been synthesized and does not account for a voltage drop in series-connected luminares. It can be seen that the input current of the power supply concept ripples around the specified target value of $I_{CD,max} = 350\,\text{mA}$. In case of lighter loads on the output of the flyback converter, significant input current is only drawn for part of the the HC phase but with the same current level. It should be noted that the limit of $I_{CD,max} = 350\,\text{mA}$ is slightly exceeded for higher loads but the input current always remains below 400 mA, which is the minimum current carrying capacity for DLT luminaires during the HC supply interval. This overstepping originates from the adjustment of the current limiter activation level, which must not be set too low. For an industrial target implementation the activation limit of the current limiter and the target input current of the boost converter have to be slightly adjusted to fully comply with the DLT specification [1].

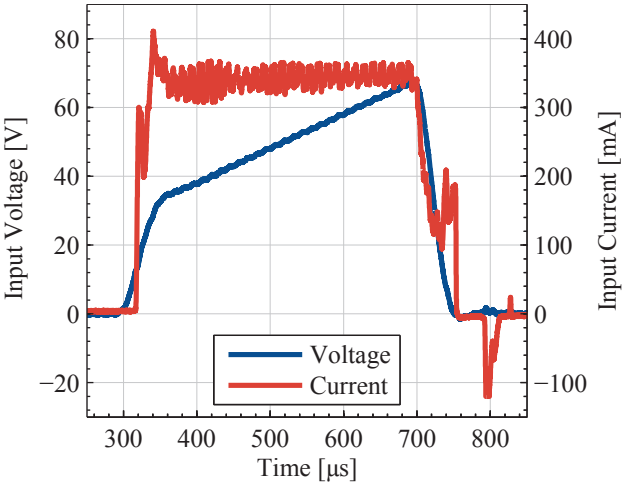


Fig. 7. Measured input characteristics at $I_{load} = 125\,\text{mA}$ and $V_{out} = 3.3\,\text{V}$.

Since the boost converter is purpose-designed for the implemented power supply, it shall be analyzed in further detail to optimize the available output energy. Fig. 8 shows the efficiency of the boost converter versus load current for different constant input voltages and switching frequencies.

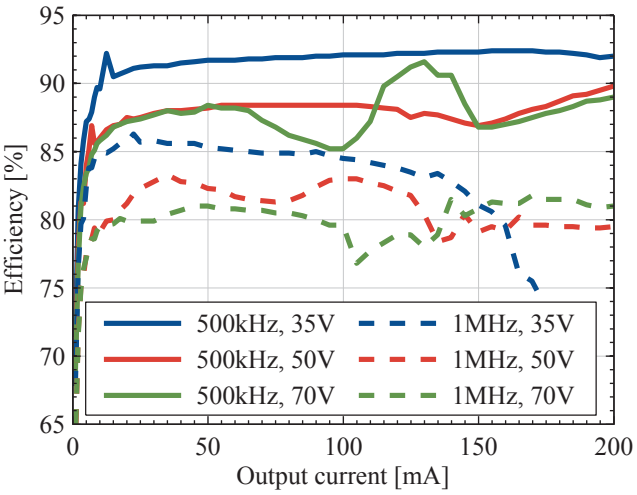


Fig. 8. Measurement on the effects of switching frequency and input voltage on boost converter efficiency.

Although the switching frequency should be as high as possible to minimize the input current ripple, the dynamic power losses have to be considered. Fig. 8 shows the significant impact of the dynamic losses. With a switching frequency of $f_{sw,boost} = 1\,\text{MHz}$ the converter efficiency is between 5 % and 10 % lower compared to identical scenarios with

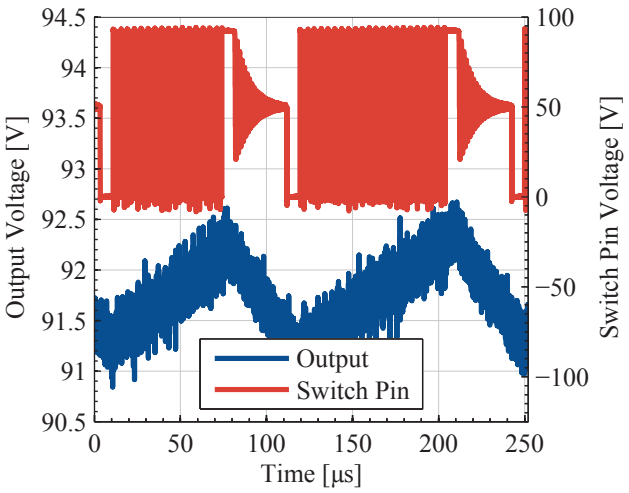


Fig. 9. Measured output and switch pin voltages of the developed boost converter for a constant 100 mA load.

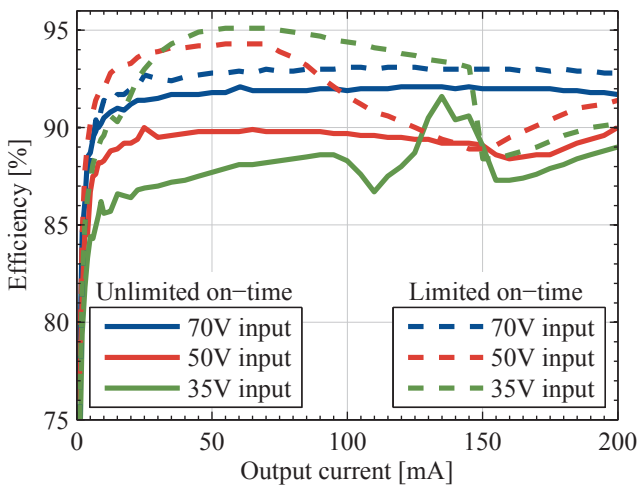


Fig. 10. Measured boost converter efficiency dependent on load current for different input voltages.

$f_{sw,boost} = 500\,\text{kHz}$. For the presented implementation a switching frequency of $f_{sw,boost} = 500\,\text{kHz}$ has thus been selected. In fact, the usage of this lower frequency even leaves some headroom for optimization as the μC can run at a lower clock frequency, reducing its power consumption. In consequence, the μC clock frequency has been lowered from 8 MHz to 1 MHz.

Fig. 9 presents output and switch pin voltage of the developed boost converter for a constant current load of 100 mA. It is clearly shown that the storage voltage ripples around its target value $V_{store,max} = 91.7\,\text{V}$. This waveform originates from the overvoltage protection circuit. The converter stops operating when the output voltage exceeds $V_{store,max}$ and starts operating again when it has dropped below this threshold. The large ripple is caused by the hysteresis of the comparator and the delays introduced by the software running on the μC.

To evaluate the performance of the proposed concept, efficiency measurements have been taken in dependency of the load current. Fig. 10 and Fig. 11 show the measured efficiencies of the individual converters with constant supply voltages applied to their inputs. The boost converter's efficiency was measured with the μC running at 1 MHz for both variants shown in Fig. 5. It can be seen that the variant with limited MOSFET on-time has significantly higher efficiency especially at light loads. Fig. 10 shows a significant improvement compared to the efficiency measured with the controller running at 8 MHz from Fig. 8. For all different input voltages the boost converter provides a quite good efficiency. The efficiency of the flyback converter on the contrary is rather poor. Especially for high input voltages and under light load conditions the flyback efficiency drops significantly. One reason for this might be that the applied IC uses an internal transistor with a relatively high resistance. Choosing a different off-the-shelf flyback IC or developing a custom-designed switching power supply for the second stage might be possible solutions to further increase efficiency and hence boost the available output power.

Fig. 12 presents the measured overall efficiency of the developed power supply concept with an output voltage of 3.3 V

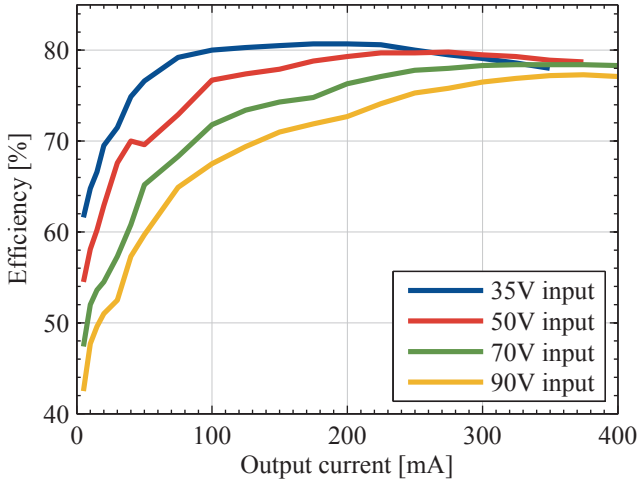


Fig. 11. Measured flyback converter efficiency at $V_{out} = 3.3\,\text{V}$ dependent on load current for different input voltages.

and the specified DLT supply voltage waveform without drop as illustrated in Fig. 1 on the input. It can be seen that the overall peak efficiency is close to the maximum considering the individual converter efficiencies measured at continuous input conditions. With regard to the very limited input power and the discontinuous conversion operation, this represents a very good result. Because the converter efficiencies multiply, even individual converter efficiencies close to 90 % would only result in a combined efficiency of about 80 %. Furthermore, the high voltage ratio between V_{store} and V_{out} limits the achievable efficiency. Nevertheless, it is expected that efficiency can be further increased by replacing the second converter stage as mentioned above. For the presented approach, an overall peak efficiency of $\eta_{peak} = 66.8\,\%$ is achieved while a maximum output power of $P_{out,max} = 3.3\,\text{V} \cdot 144\,\text{mA} = 475\,\text{mW}$ can be provided continuously. For lower load cases the efficiency drops drastically, but since this does not affect the amount of power available from the power supply, it is not relevant for

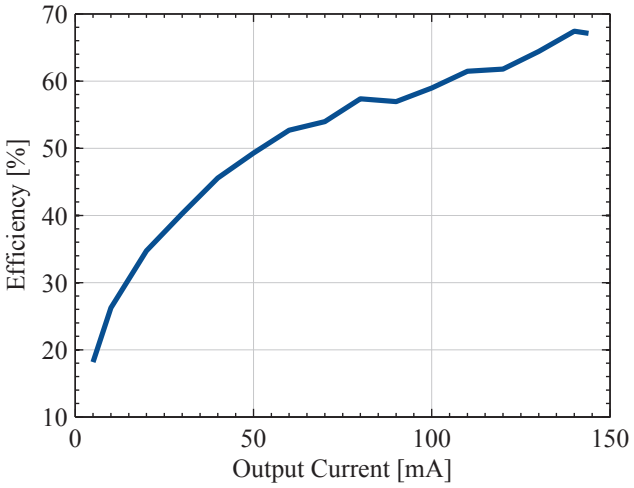


Fig. 12. Measured overall efficiency of the proposed concept at $V_{out} = 3.3\,\mathrm{V}$ dependent on load current.

the described application. The power dissipation due to this low efficiency is insignificant compared to the power draw of a typical LED luminaire.

In conclusion, the provided output power is by far high enough to run a WiFi module in all relevant modes of operation. The power supply has been tested in a real setup with a DLT compatible luminaire and has proved to work reliably over a long period of time. Even if a 20 V drop over a DLT luminaire occurs and thus drastically reduces the available energy to the control device, the harvested energy stored in C_{store} is still high enough for the occasionally occurring transmit phases of the WiFi module in its power-save mode. To ensure that WiFi association works with the full 20 V drop, a battery or dual-layer capacitor could be used to provide the required energy. This storage device can be recharged slowly with the spare input power while the WiFi module is idle in power-save mode.

In fact, this outstanding result even leaves some headroom for installing an LCD with a low-power backlight or other user interfaces, even if halfwaves of mains are missing or short blackouts of several halfwaves occur.

V. Conclusion and Outlook

This paper proposes an AC-DC power supply for DLT compatible control devices in intelligent lighting systems with high output power. The presented topology works without a neutral wire connection and is hence applicable to all typical house installations lacking a neutral wire at the light switch lead-out. A continuous output power of 475 mW is achieved at $V_{out} = 3.3\,\mathrm{V}$ and with an overall peak efficiency of 66.8 %. Drawn peak power may be much higher due to the stored energy on the capacitor C_{store}. It is shown that the provided output power is not only high enough to ensure operation of a WiFi module [2] in its power-save mode, but also during the power-hungry association phase, if the voltage drop at the luminaire during the DLT supply period is not too high.

For future work, it might be interesting to investigate an improved solution for the second converter stage, e.g. an optimized buck converter, to further increase efficiency. Nevertheless, the proposed power supply topology is an excellent solution for providing continuous operation of a DLT control device with WiFi, even if halfwaves of mains are missing or short blackouts of several halfwaves occur. In this way, DLT control devices can be embedded in a smart home environment, which is a unique feature enabled by the proposed power supply concept.

Acknowledgment

This work has been funded within the ”EnLight - Energy efficient and intelligent lighting systems” project by the ENIAC Joint Undertaking (project ID: 270707-2) and the German Federal Ministry of Education and Research (FKZ: 16N11438, Subproject: Erforschung von Elektronikbausteinen für energieeffiziente, intelligente Beleuchtungssysteme).

The authors would especially like to thank the company Insta Elektro GmbH, Lüdenscheid, Germany and Mr. Friedhelm Holtz for their continuous support and fruitful discussions.

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