# Implementation of a Wireless ECG Acquisition SoC for IEEE 802.15.4 (ZigBee) Applications

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***Abstract*—This paper presents a wireless biosignal acquisition system-on-a-chip (WBSA-SoC) specialized for electrocardiogram (ECG) monitoring. The proposed system consists of three subsystems, namely, 1) the ECG acquisition node, 2) the protocol for standard IEEE 802.15.4 ZigBee system, and 3) the RF transmitter circuits. The ZigBee protocol is adopted for wireless communication to achieve high integration, applicability, and portability. A fully integrated CMOS RF front end containing a quadrature voltage-controlled oscillator and a 2.4-GHz low-IF (i.e., zero-IF) transmitter is employed to transmit ECG signals through wireless communication. The low-power WBSA-SoC is implemented by the TSMC 0.18-$\mu$m standard CMOS process. An ARM-based displayer with FPGA demodulation and an RF receiver with analog-to-digital mixed-mode circuits are constructed as verification platform to demonstrate the wireless ECG acquisition system. Measurement results on the human body show that the proposed SoC can effectively acquire ECG signals.**

***Index Terms*—ARM-based platform, RF transceiver, SoC design, wireless ECG detection, ZigBee baseband spreading technique.**

## I. Introduction

RAPID economic and industrial development increase intensity in daily life, which results in negative sentiments, such as nervousness, anxiety, and melancholy [1]. These emotions, along with rapid lifestyle changes, result in the development of chronic cardiovascular diseases [2], which are one of the leading causes of major adult illnesses after infectious diseases [3].

Several products that aim to diagnose cardiovascular diseases have been developed in the market. For instance, BioSenseTeK promoted the EP-2000 [4], a PC-based 12-lead ECG acquisition device. North-Vision has also launched the Prince 180B [5], and IMEC has demonstrated an integrated ECG monitoring system with RF and digital signal processing capability [6]. All the above products are targeted on medical-grade ECG signal acquisition and processing capability. In addition, many studies have used the Bluetooth technology to build the ECG signal transmission network infrastructure.

System-on-a-chip (SoC) is a mainstream device because of its smaller device size, lower power consumption, and lower cost features, in which entire circuits, including digital mixed-mode (MM) signals and RF components, are integrated into a single piece of silicon [7]. The SoC developed for the body sensor network (BSN) intends to bring healthcare closer from the hospital to the patients, allowing biosignal monitoring to be conducted daily than limiting it within the clinical environment. In recent years, some wireless technologies are adopted for BSN application, such as the low-power radio frequency identification (RFID) technology [8]. These networks are also used for wireless personal area networks for the IEEE 802.15.4 standard (i.e., ZigBee applications) [9], [10]. BSN is predicted as the next homecare platform because of its significant potential as a low-cost high-patient-safety medical device [11].

Yang *et al.* [12] proposes the prototype of a biopatch with integrated low-power SoC. The SoC features the programmable gain and bandwidth for ECG detection, containing a three-stage front-end circuit, an 8-bit successive-approximation-register analog-to-digital converter (SAR-ADC), and a digital core. The SoC is integrated into a biopatch prototype without wireless transmission. Khayatzadeh *et al.* [13] presents a fully integrated wireless ECG SoC applied in a wireless body sensor network. The SoC includes a two-channel ECG front-end with an 8-bit SAR-ADC, a simple microcontroller and a SRAM, and a medical implantation communication service band RF-transceiver with binary frequency-shift keying and on–off keying (OOK) modulation for uplink and downlink transmissions, respectively. Yan *et al.* [14] proposes a low power highly sensitive ECG monitoring SoC where it is designed and implemented into a poultice-like plaster sensor for wearable cardiac monitoring. The SoC includes, four reconfigurable electrode front-ends, a differential sinusoidal current generator for balanced current injection, a digital module with finite state machine controller and SRAM data storage, and a cm-range 13.56-MHz fabric inductor coupling OOK remote communication. The SoCs implemented by both Khayatzadeh and Yan are customized as an application-specific integrated circuit (ASIC) with simple FSK and OOK wireless transmission. However, this paper presents a standard-based wireless solution (ZigBee) which has low-power consumption, low cost, high-node density, simple protocol, and long-distance communication [9]. Moreover, the spreading

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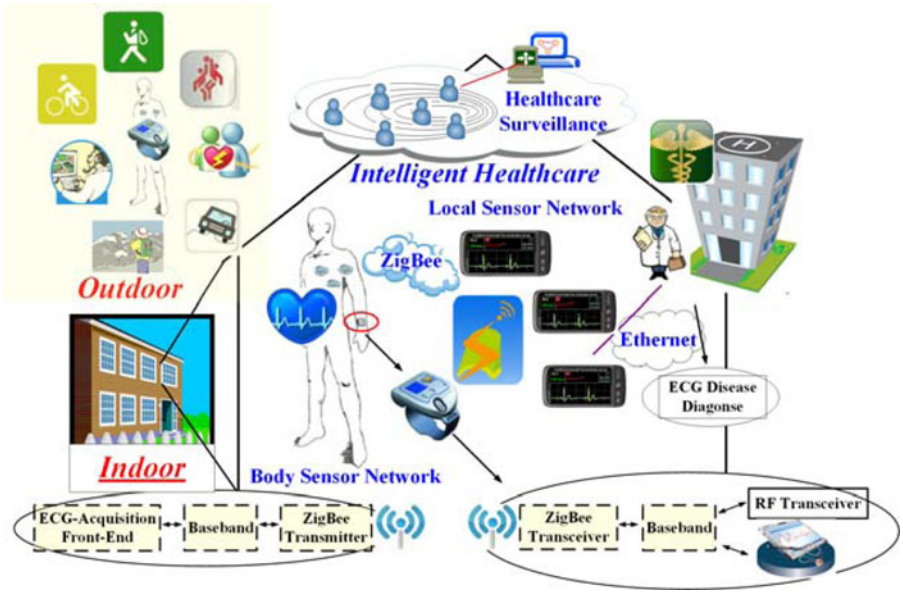


Fig. 1. Interactive intelligent healthcare and monitoring system.

technique with offset quadrature phase shift keying (O-QPSK) is adopted to decrease the noise interference.

The main contributions of the presented research are the detailed descriptions for the integrated circuit design and the measured results have revealed the achievement, different from our previous works [15] that employ an ECG acquisition module (without on-chip) and RF integrated circuits (ICs). This paper presents the first SoC with the IEEE 802.15.4 standard for wireless ECG acquisition, and aims to develop a wireless biosignal acquisition system-on-a-chip (WBSA-SoC), with on-chip ECG acquisition circuits, a baseband processor, a mixed-mode interface, and an RF transmitter, as well as an ARM-based receiver platform, to demonstrate the wireless ECG acquisition system. It makes a wearable device, but not a protocol evaluation board, to be possible in the future. The ARM-based receiver is intended for telemedical healthcare monitoring, in which, 1) the WBSA-SoC consists of an RF front-end circuit, a ZigBee transmitter baseband, and an analog front-end (AFE) circuit; and 2) the ARM-based receiver platform is constructed from an RF receiver, MM circuits, and a demodulator implemented in the FPGA with an ARM-based displayer. The rest of the paper is organized as follows. Section II presents the system architecture in personal health monitoring. Section III describes the circuit implementation of the wireless ECG acquisition system. Section IV presents the measurement results of system integration and the discussion. Section V concludes the study.

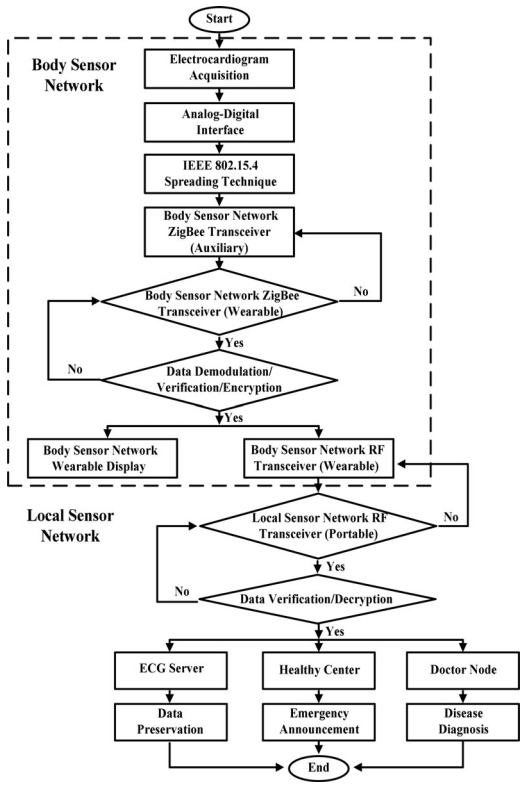


Fig. 2. Data flowchart of ECG detection for intelligent healthcare monitoring.

## II. System Architecture in Personal Health Monitoring

An interactive intelligent healthcare and monitoring system (IIHMS) [8] (see Fig. 1) is proposed to enhance the portability of home telecare system. The IIHMS includes a BSN and a local sensor network (LSN). The BSN is the medium of communication between the acquisition auxiliaries and the wearable device (e.g., watch). The auxiliary with electrical leads and WBSA-SoC are responsible for ECG signal acquisition. The LSN is the intermediate medium between the wearable device and the portable facility (e.g., mobile phone and personal digital assistant) for simple data analysis.

Fig. 2 shows the data flow of ECG signal detection for the intelligent healthcare monitor. The ECG signal is acquired by

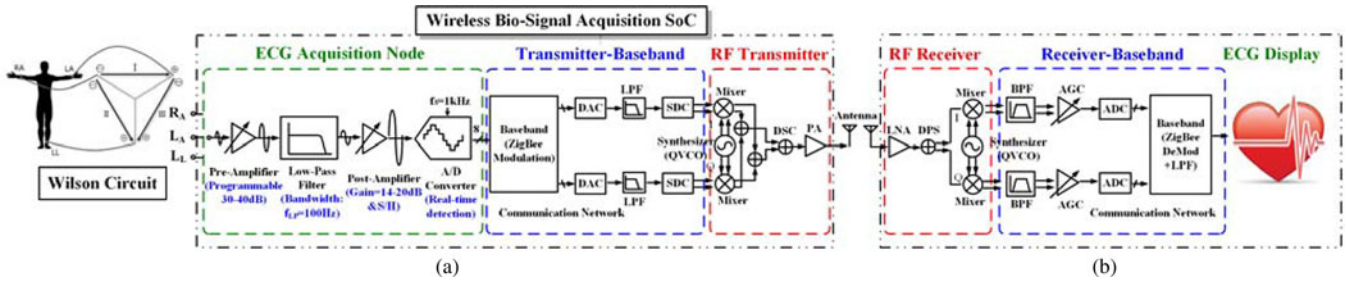


Fig. 3. (a) Block diagram of the proposed WBSA-SoC, and the (b) wireless receiver for ECG monitoring.

the WBSA-SoC. The SNR of the ECG data is improved via the ZigBee spreading technique after signal digitization. The ECG data are both demodulated and verified. If the data are correct, the ECG waveform will be displayed through the wearable device. The data are also encrypted to ensure highest confidentiality before transmittal to the portable facility. The LSN supplies the surveillance service, including data analysis and healthcare monitoring, via the ECG server and health center, respectively. Illness diagnosis is also an important service by the doctor node in the LSN.

## III. Circuits Implementation of WBSA-SoC and Receiver Platform

In this paper, the ECG acquisition circuits, a transmitter-baseband processor, and an RF front-end transmitter are used to coordinate with the low-power high-integration WBSA-SoC. The WBSA-SoC is responsible for acquiring feeble ECG signals perceived from the electrode leads [16]. The system block diagram is shown in Fig. 3(a). A real-time ECG data receiver is integrated on the board to receive and display the physical signals controlled by the ZigBee firmware. These physical signals include those from RF receiver circuits, the analog-to-digital MM interface, the demodulator implemented by FPGA, and the ARM-based displayer [see Fig. 3(b)]. The detailed circuits are described in the subsequent sections.

### A. ECG Acquisition Node

The ECG signals obtained are translated by Wilson resistors. Aside from the Wilson resistors, the AFE circuits integrate several components, including a programmable gain preamplifier (PGA), a low-pass filter (LPF), a postamplifier (PostAmp), and an analog-to-digital converter (ADC) [7]. The detailed circuit implementations are as follows:

*1) Programmable Gain Preamplifier:* The structure of the differential difference amplifier (DDA) [17] is used for the first stage of the preamplifier (PreAmp). The proposed closed-loop PreAmp comprises a DDA amplifier and a PGA to determine the functionality of the variable gain. The output gain of the PGA circuits is adjusted through the ratios of capacitance $C_i$ and $C_f$ [7], which are placed on the dc feedback path. The gain can be programmed between 30 to 40 dB.

*2) Fourth-Order Butterworth LPF:* The large magnitude of the cardiogram R and T waves can be adopted to detect cardiac diseases [18]. Therefore, an LPF with fourth-order Butterworth topology behind the PreAmp is provided to decrease the out-of-band high-frequency noise. The ladder structure [7], including resistors and inductors, can be substituted with operational transconductance amplifiers in the form of a gyrator by component replacement [19].

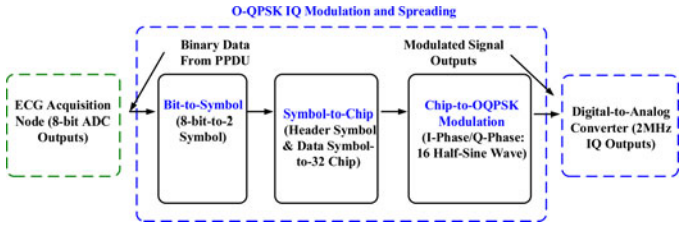


Fig. 4. Block diagram of the modulation functions.

*3) Second-Stage PostAmp:* Given the gain attenuation of the LPF and the gain-amplifying insufficiency of the PreAmp, the second-stage PostAmp is used for the dynamic-range requirement of ADC behind the PostAmp [7].

*4) 8-bit Successive Approximation ADC:* Using the high-speed ADC to digitize the ECG signal in physiology examination is unnecessary because the bandwidth of the biosignal is below 250 Hz [16]. An 8-bit successive approximation (SA)-ADC with 1-kHz sampling frequency is used to digitize the ECG signal [7]. The digital-to-analog converter (DAC) structure with a binary searching algorithm not only dominates the accuracy of the digitization but also influences the operation speed of the SA-ADC.

### B. Transmitter-Baseband Processor

The IEEE 802.15.4 specification provides the worldwide standard, operated in an unlicensed 2.4-GHz ISM band. The O-QPSK modulation with chip rate and data rate of 2 MHz and 250 kbps, respectively, is used to determine the transmitter-baseband protocol of the proposed WBSA-SoC. The MM circuits are the interface between the ZigBee digital processor and the RF front-end circuits, including a DAC, an LPF, and a single-end to differential converter (SDC) to convert the in-phase (I-phase) and quadrature-phase (Q-phase) signals into quadrature signals.

*1) ZigBee Modulation and Spreading Technique:* The ZigBee physical layers (PHYs) in the 2.45-GHz band utilize 16-ary quasi-orthogonal modulation. Four data bits are selected from one of the 16 nearly orthogonal pseudorandom noise (PN) sequences [9]. Fig. 4 shows that the corresponding modulation

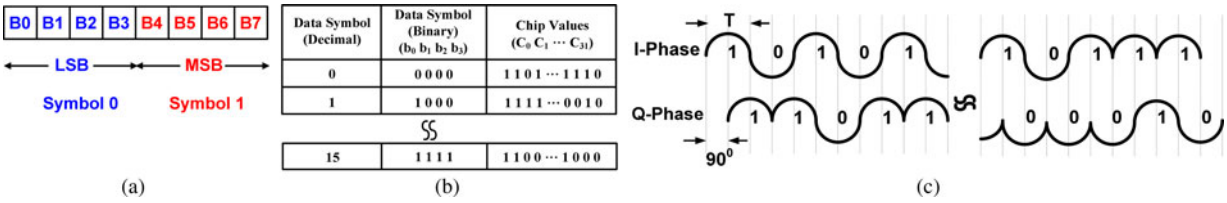


Fig. 5. (a) Bit-to-symbol mapping; (b) table of symbol-to-chip mapping; (c) samples of I-phase and Q-phase chip sequences with pulse shaping.

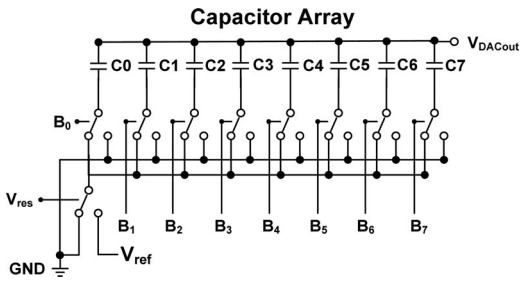


Fig. 6. Schematic of an 8-bit capacitor array DAC.

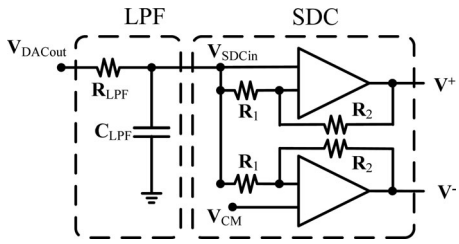


Fig. 7. Schematic of an LPF and an SDC.

and spreading techniques of the PHYs are bit-to-symbol, symbol-to-chip, and chip-to-O-QPSK carrier.

The digitized data converted from the SA-ADC of the WBSA-SoC are parallel 8-ary binary codes, which are mapped into two data symbols, such as the 4-bit least significant bit ($B_0$, $B_1$, $B_2$, $B_3$) symbol and the 4-bit most significant bit ($B_4$, $B_5$, $B_6$, $B_7$) symbol. The symbol segments are compliant with the PHY protocol data unit (PPDU) encoding specification. Fig. 5(a) shows the PPDU data symbols. Each octet data is processed beginning at the preamble bit and ending at the last PHY service data unit bit.

Each data symbol is spread into 32-chip PN sequences by using the mapping table according to the ZigBee protocol [9]. The simple mapping table is illustrated in Fig. 5(b). The chip sequences are modulated onto the carrier to employ the O-QPSK with half-sine pulse shaping. Moreover, the I-phase and Q-phase modulation carriers are constructed from the even-indexed and odd-indexed 32-chip PN sequences, respectively. Fig. 5(c) shows the pulse shaping of the I-phase and Q-phase. The Q-phase is delayed by 90° from the I-phase. The formula for half-sine pulse shaping is derived by using

$$p(t) = \begin{cases} \sin\left(\pi \dfrac{t}{T}\right), & 0 \le t \le T \\ 0, & \text{otherwise} \end{cases} \tag{1}$$

where $T$ is the period of each half-sine pulse shaping.

*2) MM Circuits:* MM circuits are responsible for translating digitized data into analog signals so that the modulated data can be transmitted via wireless transmission.

*Capacitor-Based DAC:* The DAC converts an abstract finite-precision time series data (i.e., fixed-point binary number) into a continually varying physical quantity (e.g., a voltage). The capacitor-based DAC (see Fig. 6) uses an op-amp-free capacitor array to implement a low-power DAC circuit. The output voltage with a binary-weighted capacitor array is derived by using

$$V_{\text{out}} = V_{\text{ref}} \frac{C_i + \sum_{j=i+1}^{8} B_j C_j}{C_{\text{total}}} \tag{2}$$

where $V_{\text{ref}}$ and $V_{\text{res}}$ are the DAC output swing and the dc offset voltage, respectively; $C_{\text{total}}$ is the total capacitance of the DAC; the parameter $i$ ranges from 0 to 7, corresponding to the 8-bit DAC.

The unit capacitor $C_0$ is designed to be as small as possible to minimize power consumption. However, this capacitor will be traded off with the mismatch in layout caused by process variation and the switch thermal noise in the switched-capacitor circuits. A metal–insulator–metal capacitor of 100 fF with a common-centroid matching skill has been used to tradeoff between power consumption and noise contribution. The other capacitors, $C_1$ to $C_7$, are multiples of $C_0$ and are arranged in parallel for better placement, thus avoiding matching errors.

*LPF and SDC:* Given that the output of the capacitor-based DAC resembles a staircase, an LPF is required to smoothen the waveform. An SDC is also used to provide gain and differential output for the mixer requirement. The detailed circuits are shown in Fig. 7.

### C. RF Transceiver

An RF transmitter, including a fully differential up-conversion mixer, a two-stage power amplifier, and a quadrature voltage-controlled oscillator (QVCO), is implemented and integrated in WBSA-SoC for the ZigBee system. A low-power zero-IF RF receiver, including a current-reused low-noise amplifier (LNA) and a folded-cascode down-conversion mixer, is also utilized to receive ECG signals by wireless communication according to the IEEE 802.15.4 standard. The details of the circuits are described subsequently.

*1) RF Transmitter:* The RF transmitter [15], which is used to convert the baseband signals to RF carrier for wireless transmission, is located behind the MM circuits of the WBSA-SoC. The quadrature baseband signals are converted into differential RF

signals by using the proposed up-conversion mixer. Circuit linearity results in interference in the adjacent channel; therefore, the technique of the multitanh circuit is employed to improve linearity. The common-source amplifier with two-stage cascade structures is utilized in the power amplifier to improve conversion gain and to enhance the isolation between the output and input stages. The differential pair with an active current mirror is used as an active RF-balun to transform the differential output of the up-mixer into the single-ended input of the power amplifier.

The QVCO with subharmonic and injection-locked (SHIL) techniques is applied for I/Q channel digital communication to generate quadrature outputs (0°, 90°, 180°, and 270°). The NMOS and PMOS cross-coupled pair transistors with current-reuse technique are used in the proposed SHIL-QVCO [20] to save half of the dc current and to enhance the conversion gain under the push–pull operation. NMOS frequency-doubled differential pairs provide double resonant frequency injection into the NMOS and PMOS cross-coupled pairs to lock the quadrature phase. Instead of using the traditional transformer-coupling [21], the proposed SHIL-QVCO can be used to save chip area.

*2) RF Receiver:* The architecture of direct conversion (i.e., zero-IF) is widely used in RF receivers because it does not require off-chip components to eliminate an image signal. The proposed current-reused folded RF receiver consists of a single-ended LNA, a current-reused differential power splitter (DPS), and the folded structure quadrature mixer [15]. The DPS not only provides conversion gain but also acts as an SDC between the LNA and the quadrature mixer.

With regard to power gain, the gain efficiency of the proposed LNA can be increased by biasing the transistors in the subthreshold region. In this paper, a DPS circuit [15] stacked on the single-ended LNA for current reuse is directly implemented without extra power consumption. According to the Friis equation [22], the thermal noise of a mixer can be sufficiently suppressed by the LNA and DPS with high conversion gain. Moreover, the flicker noise can be reduced simultaneously because of its large transistor size in the subthreshold region.

### D. Receiver Baseband and ARM-Based Displayer

The receiver baseband is divided into two parts 1) the analog-to-digital MM board, which is constructed with bandpass filter (BPF) circuits, an automatic gain-controlled amplifier (AGCA), and a 10-bit ADC; and 2) the O-QPSK digital demodulation implemented in FPGA and ARM-based displayer for demonstrating the ECG waveform. The system block diagram of the receiver baseband is shown in Fig. 8, and the details of the circuit integration are described subsequently.

*1) Analog-to-Digital MM Board:* BPF is employed as the first stage of the MM circuits to reject out-of-band noise, which is implemented by a second-order high-pass filter with bandwidth of 30 kHz combined with a first-order LPF with bandwidth of 280 kHz. The BPF is used not only to amplify the tiny quadrature baseband signal but also to convert the differential

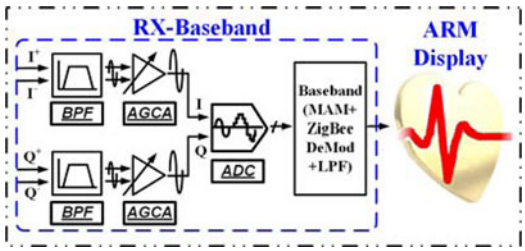


Fig. 8. Block diagram of RX-baseband circuits.

input to the single-ended output. An AGCA is used behind the BPF to satisfy the dynamic voltage of an ADC. The IA model, INA217, which has low dc supply voltage and wide operation bandwidth, is suitable to function as the required AGCA.

The ADC selected in the MM board should have low dc supply voltage, low power consumption, and high bit resolution. The AD9201 with a dual channel and a 10-bit resolution is used to provide the quadrature I/Q channels for digital communication. The rising and falling edges of the clock in ADC are applied to convert the I-phase and Q-phase signals to the digital codes simultaneously.

*2) O-QPSK Digital Demodulation:* Both dual 10-bit I/Q channel digitization codes are demodulated in FPGA. Fig. 9(a) shows the procedures of the digital demodulation. The digitized data with noise interference are precisely converted from the ADC circuits and stored in the registers embedded in the FPGA. The data prefiltered before the I/Q chips are demapped. A conventional moving average method (MAM) is also used to modify the waveform distribution and to enhance data identification. Fig. 9(b) shows the analog waveform at the output of the ModelSim simulator with AD9201 (i.e., ADC_$I_{out}$ and ADC_$Q_{out}$). High noise interference is injected into the I/Q half-sine pulse shaping [see Fig. 9(b)]. However, according to the filtering and MAM technique, the I/Q waveform can be exactly recovered (i.e., MAM_$I_{out}$ of MAM_$Q_{out}$) and demapped as I/Q chip values, as shown in Fig. 5(c).

The configuration of the I/Q chip values includes a leading header and the ECG data. The MM board with a LabView simulator is used to preverify the demodulation in the FPGA. Through the LabView simulator, the demodulation data without header data can demonstrate the ECG waveform [see Fig. 9(c)]. Given the 60-Hz instrument noise interference, a 256-tap finite impulse response LPF is adopted to filter the 60-Hz noise. The ECG signals at the Pre_LPF and Post_LPF outputs in Fig. 9(c) describe the ECG waveform with and without 60-Hz noise interference, respectively. The ECG signal can be further processed by digital signal processing in software [23] or hardware [24] to realize the anomaly detection, feature extraction, or classification.

## IV. Experimental Results and Discussion

The proposed low-power high-integration WBSA-SoC, including the ECG acquisition node, a transmitter-baseband digital I/Q modulator, and an RF front-end transmitter, is

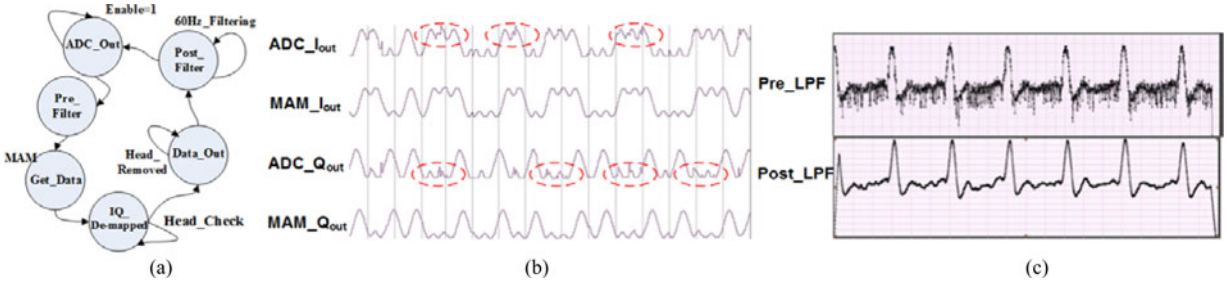


Fig. 9. (a) Procedure of IQ demodulation, (b) data out of ADC_IQ and MAM_IQ, and (c) ECG output of Pre_LPF and Post_LPF.

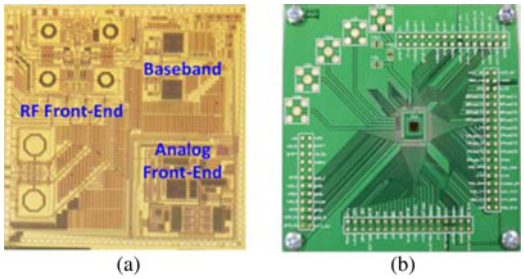


Fig. 10. (a) Chip microphotograph and (b) daughter board of WBSA-SoC.

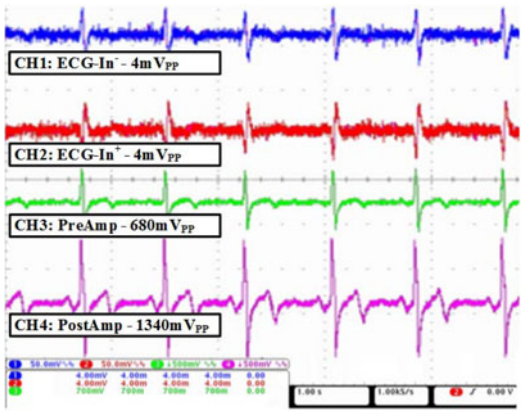


Fig. 11. Measurement results of AFE circuits on an actual human body.

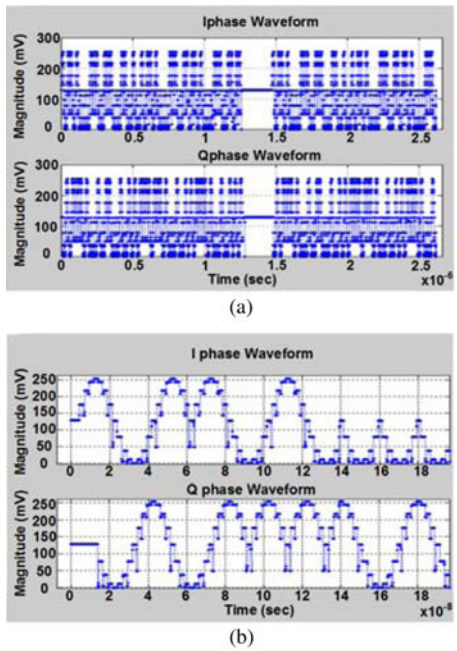


Fig. 12. (a) I/Q modulation waveform recovered by logic analyzer and MATLAB simulators; the (b) 90°-phase difference between I-phase and Q-phase.

implemented in the TSMC 0.18-$\mu$m standard CMOS process, moreover, the ASIC is the first full function SoC applied in wireless ECG detection in the word. The die area of the WBSA-SoC is 9 mm$^2$, as shown in Fig. 10(a). The WBSA-SoC hollowed wire bond onto the PCB with gilding is used to replace the traditional ceramic package in ECG examination. The daughter board is shown in Fig. 10(b).

Fig. 11 shows the measurement results obtained by the AFE circuits during human-body ECG detection. The results are measured from each output node of the following AFE circuits: 1) the measured ECG waveform (see Fig. 11: ECG_In$^{+/-}$), which is the amplitude of the R-Wave and S-Wave interval (R–S interval, approximated to 4 mV$_{\mathrm{R\text{-}S}}$); 2) the output of the PGA and PostAmp. Fig. 11 shows the PreAmp and PostAmp, whose amplitudes of the R–S interval are approximately 680 and 1340 mV$_{\mathrm{R\text{-}S}}$, respectively. The corresponding conversion gains are 44.6 and 50.5 dB, respectively.

The Agilent 16901A logic analyzer is used to measure the dual I/Q channel modulation data converted from the ADC of WBSA-SoC. Moreover, the MATLAB simulator is used to recover the digitized data as analog signals. Fig. 12(a) shows the half-sine pulse shaping of the I/Q-phase dual channels. The phase difference between the dual channels (I-phase leading Q-phase 90°) is fitted in the ZigBee specification [8]. Fig. 12(b) illustrates the O-QPSK digital modulation. According to the measured results, the current consumption of analog front-end and digital I/Q channels are 0.74 and 0.29 mA, respectively, under the supply voltage of 1.8 V.

The DAC is applied to translate the O-QPSK modulation codes into analog signals. Fig. 13(a) shows the I/Q-phase modulation waveforms converted from the DAC circuits of WBSA-SoC. Fig. 13(b) shows the measured differential modulated waveform of the I-phase ($I^+$ and $I^-$). Furthermore, the four quadrature signals of the I/Q channels ($I^+$, $I^-$, $Q^+$, and $Q^-$) are injected into the up-conversion mixer and mixed with the local oscillation frequency provided by the proposed QVCO.

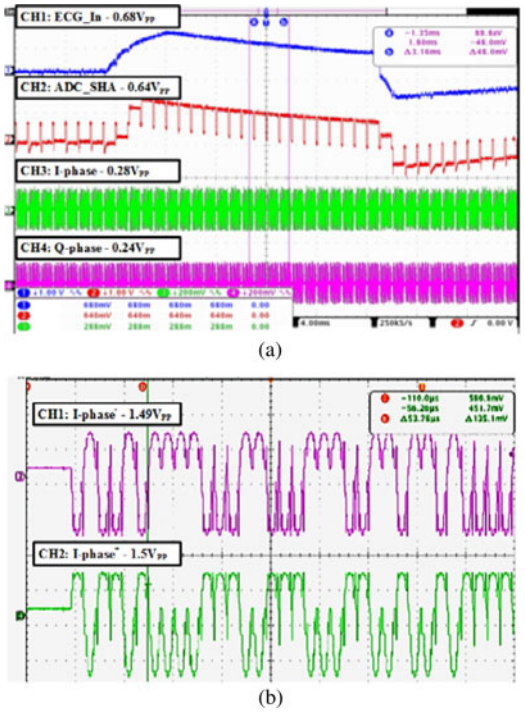


Fig. 13. (a) Outputs of AFE circuits and DAC; (b) the I-phase differential waveform of DAC outputs.

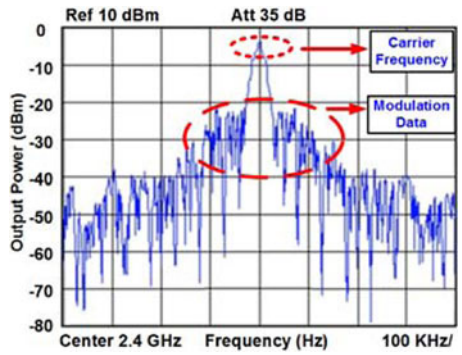


Fig. 14. Transmitter output power measured with a power spectrum analyzer.

The transmission power of the RF transmitter of WBSA-SoC is measured by using a power spectrum analyzer, as illustrated in Fig. 14, in which the carrier frequency and data bandwidth are 2.4 GHz and 200 kHz, respectively. The current consumption of MM circuits and RF-transmitter are 0.69 and 19.38 mA, respectively, under the supply voltage of 1.2 V. Therefore, the total current consumption of WBSA-SoC neglecting regulator circuits is 21.1 mA. Fitted with two 605 mAh PR44 zinc-air batteries, the WBSA-SoC can be operated for over 2 days. Fig. 15 describes the received power spectrum with I/Q channel modulation data from the down-conversion mixer of the RF receiver under 15 cm distance in the air. The data curve decreases slowly and significantly until the frequency band becomes larger than 2.6 MHz. The highest amount of data is obtained theoretically in the range 150 to 750 kHz, where the scale of the $x$-axis of the power spectrum analyzer is 650 kHz.

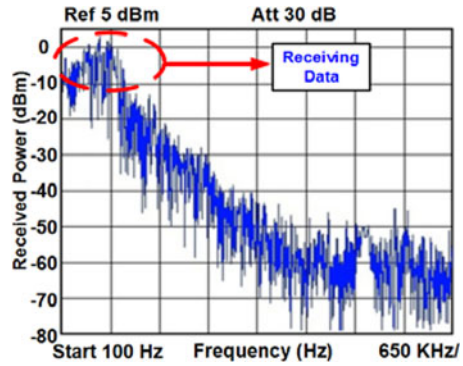


Fig. 15. Received signal power measured by using a power spectrum analyzer.

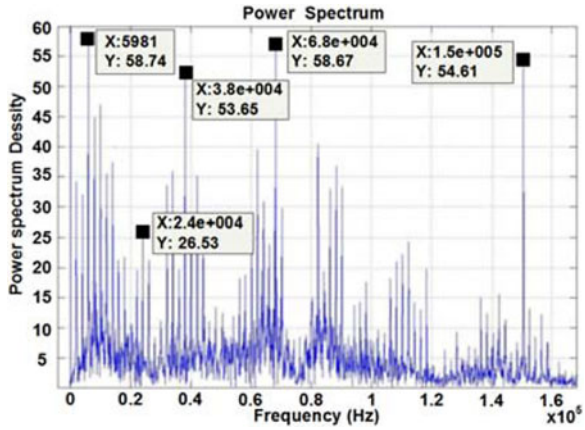


Fig. 16. Spectrum of the received data processed with a MATLAB simulator.

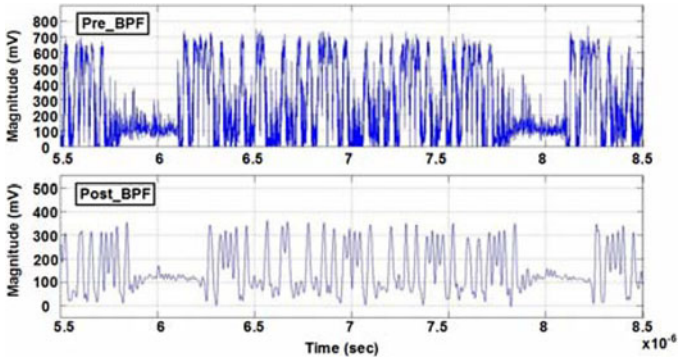


Fig. 17. Received data for pre-BPF and post-BPF.

To observe the data distribution, the MATLAB simulator with fast Fourier transform algorithm is applied to translate the received data from the time domain to the frequency domain. Fig. 16 shows that the bandwidth of the modulation data is less than 250 kHz, and the data distributed beside the 250 kHz are harmonic signals and high frequency interference.

The BPF behind the RF down-conversion mixer is utilized not only to filter high-frequency noise but also to block the dc feedback punched through the RF receiver. Fig. 17 shows the modulation data with or without high-frequency interference (Pre_BPF/Post-BPF). This figure reveals that the signal is clear with the BPF in place.


Fig. 18. (a) Experiment environment setup; (b) measurement result by an actual human body; (c) ECG biosignal display in the ARM-based displayer.

ECG detection is implemented in the WBSA-SoC daughter board, which is mounted on the fully integrated motherboard [see Fig. 18(a)]. The human-body ECG acquisition signal is translated from the Wilson resistors with electric patches stuck on the right wrist, left wrist, and left ankle. The oscilloscope is used to preshow the ECG signal in each output of the AFE circuits, including the automatic gain-controlled PreAmp and PostAmp. The human ECG detection is illustrated in Fig. 18(b). Once the ECG signal is acquired and digitized, the data are modulated and transmitted by the proposed WBSA-SoC. If the radiation carrier is received from the ARM-based receiver platform, the signals are processed by the MM circuits with amplification and digitization, the FPGA with demodulation, and the ARM-based display. Fig. 18(c) shows the ECG waveform presented by the ARM-based displayer.

The ECG experiment is validated by applying several types of daughter boards for auxiliary system integration. In this setup, 1) a bias board instead of a power supply provides all the required dc voltage of the system, and the bias circuits can be designed and integrated into the SoC in the future; 2) an off-chip clock generator provides the baseband and ADC operation frequency; 3) the level shifter and digital buffer are integrated into the motherboard to isolate the high voltage into the WBSA-SoC and to enhance the driving capability between ADC and digital modulation, respectively.

The ECG data demonstration with wireless transmission has poor reliability between the RF transmitter and receiver circuits because the noise and interference are significant during data transmission in the air. For future investigations, two approaches can be adopted to enhance the reliability of the WBSA-SoC: 1) modify the RF circuits with respect to noise isolation and increase the gain efficiency for high noise rejection; 2) use the multilayer PCB with noise shielding to improve wireless transmission.

## V. Conclusion

This paper presents an IIHMS, including a BSN and a local sensor network. The WBSA-SoC for BSN application is adopted to acquire actual human-body ECG signals via the IEEE 802.15.4 ZigBee network communication. The high-integration WBSA-SoC, including an ECG acquisition node, a transmitter-baseband processor with ZigBee protocol, an MM interface, and an RF transmitter, is implemented in the TSMC 0.18-$\mu$m standard CMOS process. In addition, an ARM-based receiver platform, which includes an RF receiver, an analog-to-digital MM board, an O-QPSK digital demodulation implemented in FPGA, and an ARM-based display, is adopted to demonstrate the wireless ECG communication. According to the actual human ECG measurement results, the ECG signals can be acquired and transmitted by using the proposed WBSA-SoC. Improving the data transmission of RF front-end circuits will enhance the noise resistance in wireless communication and increase the system performance.

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