A Wide Linear Output Range Biopotential Amplifier for Physiological Measurement Frontend

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***Abstract*— This paper presents a wide linear output range biopotential amplifier for physiological measurement frontend. The proposed amplifier consists of an open-loop rail-to-rail differential pair in the first stage and a closed-loop common source amplifier in the second stage, which extends the linear output range by maintaining a constant voltage gain with amplifier output level variation. The nMOS and pMOS gain enhancement switches provide additional compensation for the voltage gain degradation as the amplifier output level moves toward the supply rails. In addition, voltage buffers are used after the first and second stages to alleviate the loading effect. This enables using small-sized feedback resistors, where the amplifier performance is relatively insensitive to resistor mismatch. Aside from the wide linear output range, this approach leads to small silicon area, low power, and relatively high common mode rejection ratio and power supply rejection ratio, which are highly demanding for portable and implantable biomedical instrumentation frontend. The proposed amplifier is implemented using CMOS 0.35-μm technology (3.3 V supply) with core area of 0.063 mm^2. Measurement results show a stable voltage gain of 46.3 dB for amplifier output range from 0.15 to 3.12 V, and a 0.04% total harmonic distortion with input amplitude of 15 mV$_{pp}$. Furthermore, the amplifier operation is demonstrated with an actual ECG measurement setup.**

***Index Terms*— Biopotential amplifier, gain enhancement switch, low total harmonic distortion (THD), physiological measurement frontend, wide linear output range.**

I. Introduction

RECENTLY, due to the diversified needs for quality health care technologies, physiological measurement systems that can efficiently monitor the patient's biopotentials, such as ECG, EEG, and blood pressure are highly demanding [1]–[3]. Fig. 1 shows the block diagram of a physiological measurement frontend that includes the sensor electrodes, biopotential amplifier, filter, and analog-to-digital converter (ADC). The key element of the measurement frontend is the biopotential amplifier that determines the overall performance of the measurement system. To amplify weak and noisy biopotentials without loss, amplifiers require stable gain, low noise, high common mode rejection ratio (CMRR), and high input impedance. In addition, the amplifier requires a wide linear output range to maintain a high dynamic range for the measurement frontend by maximizing the input range of the ADC. The linear output range of an amplifier is defined as the output range with constant voltage gain, in other words the output range without distortion. Fig. 2 shows the amplifier transfer characteristic with a wide and a narrow linear output range. A wide linear output range is preferred, since poor amplifier output range can lead to higher ADC resolution and higher power consumption to maintain the required signal-to-noise ratio of the measurement frontend [4], [5]. The linear output range of the amplifier is critically limited by voltage gain reduction with output level variation. The gain reduction is mainly caused by output resistance variation of the output-stage transistors as the drain to source voltage change. This is much severe for cascode output stages, which will significantly reduce the linear output range of the amplifier [6]–[8]. Moreover, this will be one of the major nonidealities that will critically degrade the performance of the biopotential amplifiers as the transistor sizes continue to scale down and the supply voltage further reduces. However, not much research has been focused on improving the linear output range of biopotential amplifiers, yet a lot of research has been emphasized on reducing the input offset and noise, and improving the CMRR.

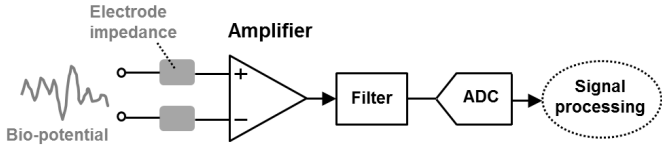

Fig. 1. Block diagram of a physiological measurement frontend.

So far, among the amplifiers, the current-mode instrumentation amplifier (CMIA) is the most widely used architecture for biopotential measurements due to low power, low noise, and high CMRR [9], [10]. Although CMIAs are widely used for biopotential amplification, to obtain a wide linear output range, an additional rail-to-rail output stage or a fully differential design is required, which can increase the power and the silicon area [11], [12]. The differential difference amplifier (DDA)-based instrumentation amplifiers (IAs) can achieve high CMRR; however, DDAs require extra circuit components, such as the class AB output stage to drive the feedback resistors and the common-mode (CM) feedback loops, which eventually leads to higher power and larger silicon area [13]–[15].

In this paper, a wide linear output range biopotential amplifier for physiological measurement frontend is proposed.

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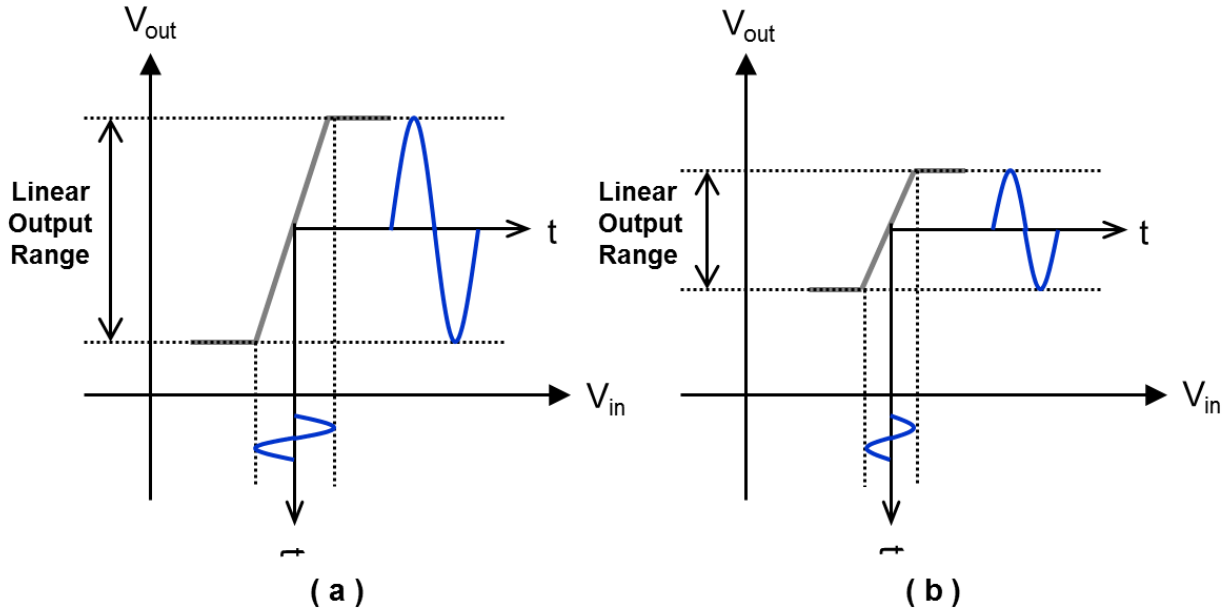

Fig. 2. Amplifier transfer characteristic with (a) wide linear output range and (b) narrow linear output range.

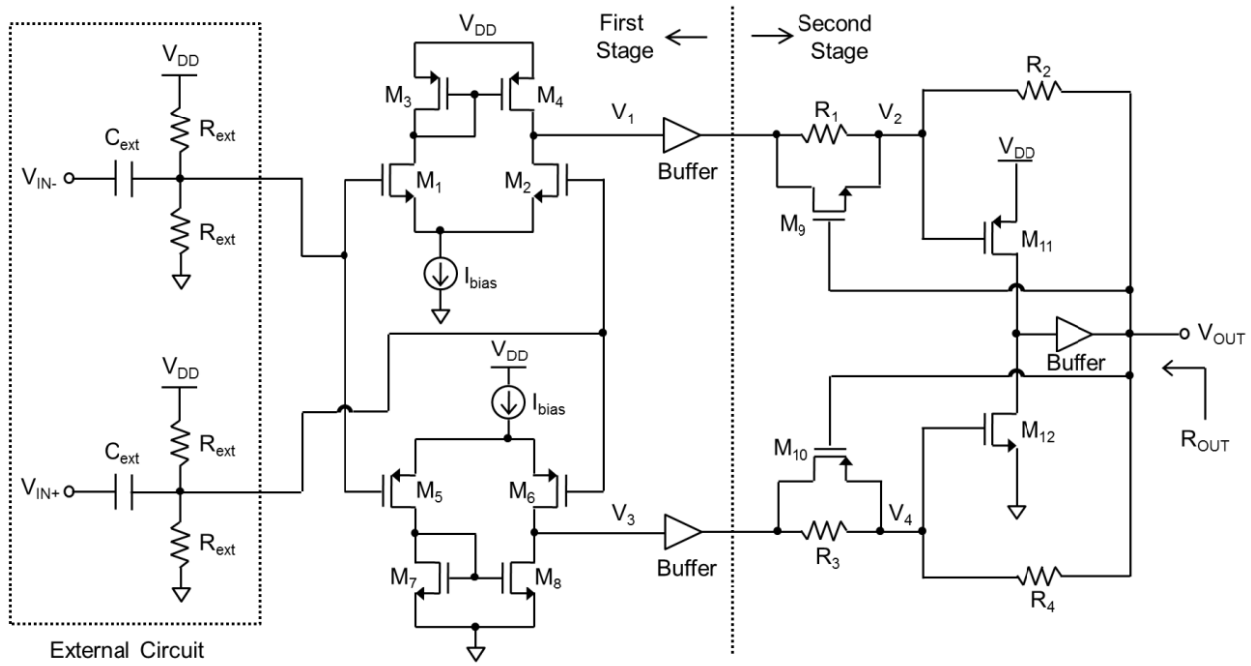

Fig. 3. Proposed amplifier architecture.

Using the first-stage open-loop and the second-stage closed-loop configuration with the gain enhancement switches, a wide linear output range can be obtained. Due to the wide linear output range, the proposed amplifier can maintain a high dynamic range for the biopotential measurement frontend. This can lead to a lower power consumption compared the biopotential measurement system proposed in [4], where the biopotential amplifier operates at a higher supply voltage than the ADC. In addition, the proposed amplifier uses a stable local feedback loop to extend the linear output range, whereas DDAs use local and global feedback loops, which require additional stability considerations. Overall, the proposed biopotential amplifier enables small silicon area and low-power operation, whereas maintaining a relatively high CMRR and power supply rejection ratio (PSRR). The remaining portion of this paper is organized as follows. The proposed amplifier architecture, linear output range extension, and frequency response are described in Section II. Noise, CMRR, and PSRR performance are addressed in Section III. Section IV shows the simulation results using biopotential signals and Section V

describes the experimental results. The conclusion is given in Section VI.

II. Proposed Biopotential Amplifier

A. Amplifier Architecture

Fig. 3 shows the proposed amplifier architecture that consists of the first-stage open-loop and the second-stage closed-loop configuration. The circuit block within the dotted line shows the external high-pass filter that is used to eliminate the dc offset originating from the skin-electrode interface. The first stage consists of the rail-to-rail differential amplifier and two voltage buffers. The second stage includes the closed-loop class-A amplifier (M_{11} and M_{12}), a voltage buffer and two gain enhancement switches (M_9 and M_{10}). As shown, the first stage is efficiently combined with the second-stage closed-loop amplifier. The first-stage nMOS input pair drives the second-stage pMOS amplifier, and vice versa, where the drain of M_{11} and M_{12} is tied together for the output generation. This eliminates using two separate second-stage amplifiers for each first-stage nMOS and pMOS input pairs, which leads to a compact amplifier architecture. The first-stage open-loop maintains a high input impedance, whereas the second-stage closed-loop minimizes the overall amplifier gain reduction with output level variation. However, due to the closed-loop configuration, the second-stage input resistance is not high. Hence, this will decrease the first-stage gain. To prevent this problem, voltage buffers are added to the first-stage output node. Another buffer placed at the second-stage output node alleviates the loading effect that enables using small-sized feedback resistors.

The operation of the proposed amplifier is divided into three regions depending on the input voltage levels $V_{\text{in}+}$ and $V_{\text{in}-}$. In case the input voltage difference is small, $V_{\text{in}+} \approx V_{\text{in}-}$, the first-stage outputs V_1 and V_3 will be in the midsupply range, which is the CM level. As a result, the second stage will not experience much gain reduction, and both gain control switches M_9 and M_{10} will be inactive. In this case, the small-signal output voltage of the nMOS input pair V_1 and the pMOS input pair V_3 can be expressed as

$$v_1 = -A_{1n} \cdot (v_{\text{in}+} - v_{\text{in}-}) \tag{1}$$

$$v_3 = -A_{1p} \cdot (v_{\text{in}+} - v_{\text{in}-}) \tag{2}$$

where A_{1n} and A_{1p} are the first-stage open-loop gain of nMOS and pMOS input pairs, respectively. Assuming the node voltages V_2 and V_4 are fixed to the CM voltage by the second-stage feedback operation, the node equation at node V_2 and V_4 can be written as

$$\frac{v_1 - v_2}{R_1} = \frac{v_2 - v_{\text{out}}}{R_2} \tag{3}$$

$$\frac{v_3 - v_4}{R_3} = \frac{v_4 - v_{\text{out}}}{R_4} \tag{4}$$

where unity buffer gains are assumed. The overall voltage gain is obtained by combining (3) and (4) with the equation relating v_{out} with v_2 and v_4, which is given as

$$v_{\text{out}} = -g_{m11}(r_{o11} \| r_{o12}) \cdot v_2 - g_{m12}(r_{o11} \| r_{o12}) \cdot v_4 \tag{5}$$

where g_{m11} and g_{m12} are the transconductance of M_{11} and M_{12}, and r_{o11} and r_{o12} are the output resistance of M_{11} and M_{12}, respectively. In addition, considering a symmetrical design, $g_{m11} = g_{m12}$, the second-stage open-loop gain is defined as

$$A_2 = -\frac{v_{\text{out}}}{v_2} = -\frac{v_{\text{out}}}{v_4} = g_{m11,12}(r_{o11} \| r_{o12}) \tag{6}$$

where the node voltages V_2 and V_4 are assumed to be identical due to the second-stage feedback operation. As a result, assuming the output resistance of the buffer R_{buff} is much less than R_1 and R_3, the overall voltage gain $v_{\text{out}}/(v_{\text{in}+} - v_{\text{in}-})$ is given as

$$A_{\text{ov}} = -\frac{\left(\frac{A_{1n}}{R_1} + \frac{A_{1p}}{R_3}\right)}{\frac{1}{(R_2 \| R_4)} + \frac{1}{A_2} \cdot \left[\frac{1}{(R_1 \| R_2)} + \frac{1}{(R_3 \| R_4)}\right]}. \tag{7}$$

Furthermore, assuming $A_1 = A_{1n} = A_{1p}$, and $R_{1,3} \ll R_{2,4}$, the overall gain can be simplified as

$$A_{\text{ov}} = A_1 \cdot A_{2,\text{cl}} \tag{8}$$

where $A_{2,\text{cl}}$ is the closed-loop gain of the second stage, $A_{2,\text{cl}} = v_{\text{out}}/v_1 = v_{\text{out}}/v_3$ that is expressed as

$$A_{2,\text{cl}} \approx -\frac{\left(\frac{R_2 \| R_4}{R_1 \| R_3}\right)}{1 + \frac{1}{A_2} \cdot \left(\frac{R_2 \| R_4}{R_1 \| R_3}\right)}. \tag{9}$$

Therefore, if $A_2 \gg 1$, A_{ov} will simply be the product of A_1 and the resistor ratios $(R_2 \| R_4)/(R_1 \| R_3)$. In case the input voltage difference is large, $V_{\text{in}+} \gg V_{\text{in}-}$ or $V_{\text{in}+} \ll V_{\text{in}-}$, node voltages V_1 and V_3 will deviate from the midsupply level, and the amplifier output V_{out} will move toward the supply rails. This will either put M_{11} or M_{12} in the triode region by reducing the drain to source voltage, which will reduce A_2. However, the gain enhancement switches M_9 and M_{10} will be activated depending on the amplifier output level V_{out}, which will modify the second-stage closed-loop gain as

$$A_{2,\text{cl}} \approx -\frac{\left(\frac{R_2 \| R_4}{R_1' \| R_3'}\right)}{1 + \frac{1}{A_2} \cdot \left(\frac{R_2 \| R_4}{R_1' \| R_3'}\right)} \tag{10}$$

where $R_1' = (R_1 \| R_{\text{ON},M9})$ and $R_3' = (R_3 \| R_{\text{ON},M10})$, and when V_{out} is near GND, M_9 will be OFF ($R_{\text{ON},M9} = \infty$) and when V_{out} is near V_{DD}, M_{10} will be OFF ($R_{\text{ON},M10} = \infty$). Therefore, R_1' and R_3' will compensate the overall gain degradation caused by A_2 reduction. For the proposed amplifier, to make $A_1 = 35$ dB and $A_2 = 30$ dB, the tail bias current of the first-stage nMOS and pMOS input pairs is set to 0.7 μA and the second-stage bias current is set to 1 μA. In addition, the size of the first-stage input devices M_1, M_2, M_5, and M_6, and the second-stage input devices M_{11} and M_{12} are set properly to obtain an identical g_m.

Fig. 4 shows the voltage buffer that includes the rail-to-rail differential pair combined with the output-stage transistors M_{9b} and M_{10b} in negative feedback configuration.

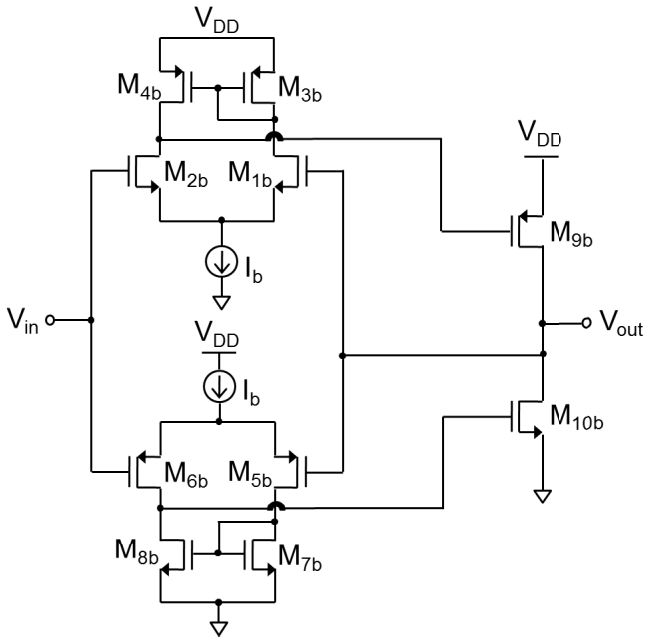

Fig. 4. Rail-to-rail voltage buffer.

The negative feedback makes the output resistance of the common source stage reduce by the factor of the feedback loop gain [16]. As a result, the output resistance of the buffer can be approximated as

$$R_{\text{buff}} \approx \frac{1}{A_{\text{diff}} \cdot (g_{\text{mb9}} + g_{\text{mb10}})} \tag{11}$$

where A_{diff} is the gain of the input differential pair. For the proposed amplifier, A_{diff} is set to 35 dB and $g_{\text{mb9,10}}$ of 15 μA/V to keep the output resistance around 550 Ω, which is less than 1/15 of the feedback resistor R_2 and R_4. Simulation results show R_{buff} of 554.6 Ω for the nominal case, and with worst-case process corners, R_{buff} changes from 495.7 to 612.8 Ω. Identical buffers are used at the first- and second-stage output nodes.

B. Linear Output Range Extension

The value of R_1, R_3 and R_2, R_4 is set to 1 and 10 kΩ, respectively. This makes the resistor ratio $(R_2 \| R_4)/(R_1' \| R_3')$ equal to 10. Furthermore, the size of the gain enhancement switches M_9 and M_{10} is set such that R_1' and R_3' vary symmetrically from 1 kΩ to 150 Ω as V_{out} varies within the output range of the amplifier. However, as V_{out} moves toward the supply rails, node voltages V_2 and V_4 deviate from the midsupply level, 1.65 V. That is, for $V_{\text{in}+} \gg V_{\text{in}-}$, V_{out} moves toward V_{DD} and node voltages V_2 and V_4 approach 0 V, which turns ON M_9 and turns OFF M_{10}. On the other hand, for $V_{\text{in}+} \ll V_{\text{in}-}$, V_{out} moves toward GND, and node voltages V_2 and V_4 approach V_{DD}, which turns OFF M_9 and turns ON M_{10}. This will cause an abrupt change in R_1' and R_3' as V_{out} approaches the supply rails due to the sudden increase in the gate to source voltage of M_9 and M_{10}. In fact, this is favorable for the overall gain linearity by providing a higher degree of compensation as A_2 drastically reduces.

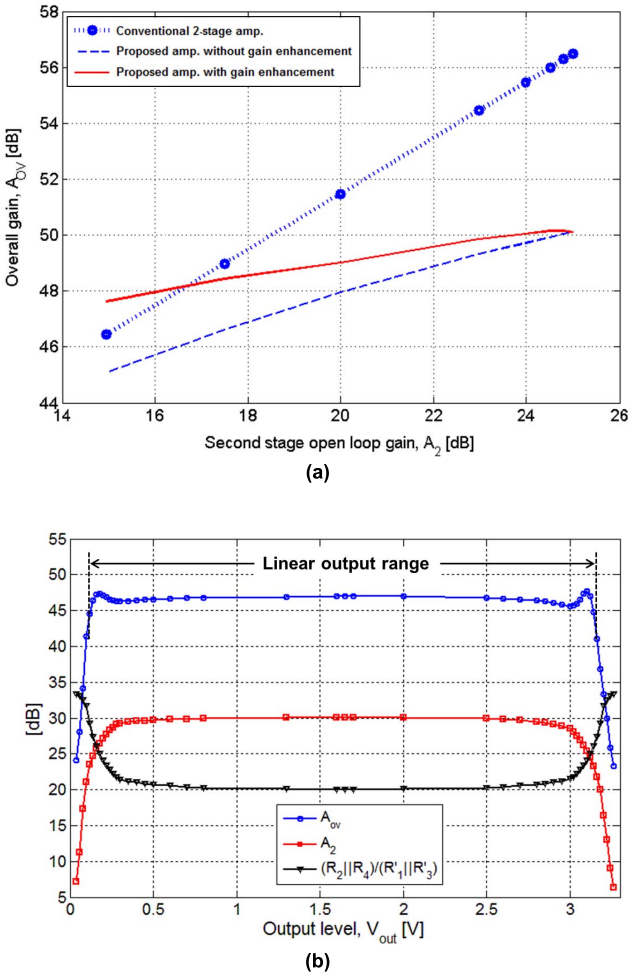

Fig. 5. (a) Overall gain variation with respect to A_2. (b) Linear output range extension with A_2 reduction.

Fig. 5(a) shows the A_{ov} variation with respect to A_2, with and without the contribution of the gain enhancement switches. The conventional amplifier refers to the two-stage amplifier with both first- and second-stage open-loop configuration [17]. The A_{ov} of the proposed amplifier without the contribution of the gain enhancement switches is obtained from (7). However, to find A_{ov} variation with the contribution of the gain enhancement switches, A_2, R_1', and R_3' values with different V_{out} levels are obtained from the circuit simulation, and A_{ov} for each V_{out} level is calculated from (8). Results show A_{ov} degradation for the conventional two-stage amplifier is linearly proportional to A_2 reduction, whereas for the proposed amplifier, A_{ov} degradation is only 5 dB (without gain enhancement) and 2.3 dB (with gain enhancement) for A_2 reduction of 10 dB. This shows A_{ov} degradation with A_2 reduction can be minimized by the operation of the gain enhancement switches, which will lead to a wider linear output range. The linear output range extension under A_2 reduction can be further described using (8) and (10). Noticing A_1 reduction is less than A_2 reduction with V_{out} level variation (since V_{out} has a wider variation range than the first-stage outputs V_1 and V_3), A_2 reduction will cause A_{ov} degradation as V_{out} move toward the supply rails. However, due to the

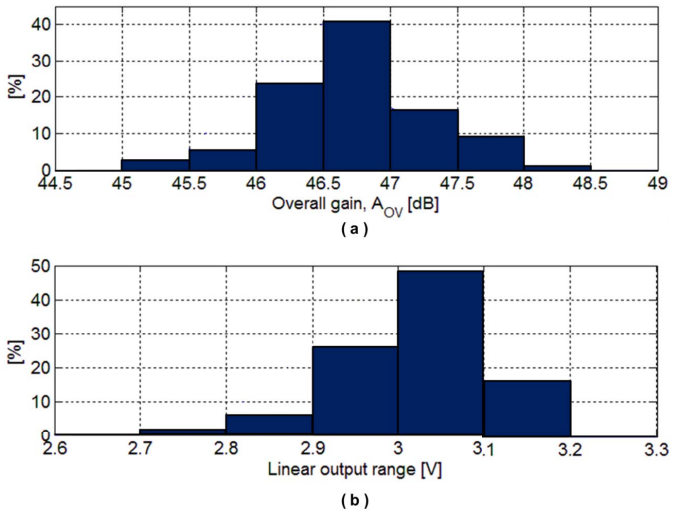

Fig. 6. Monte-Carlo simulation results. (a) Overall gain. (b) Linear output range.

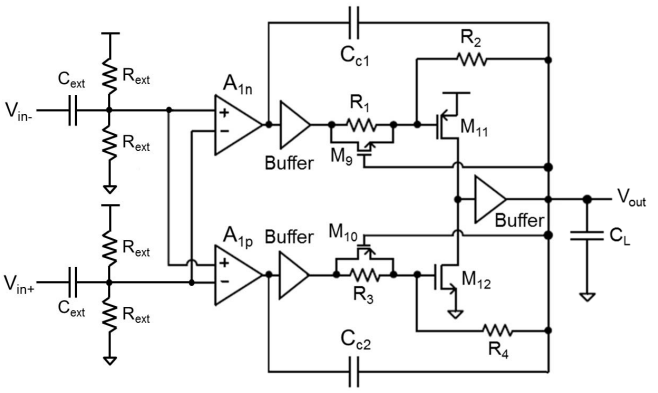

Fig. 7. Proposed amplifier with feedforward capacitors C_{c1} and C_{c2}.

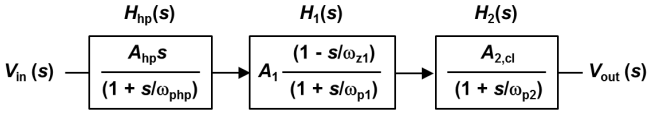

Fig. 8. Amplifier s-domain block diagram.

gain enhancement switches M_9 and M_{10}, the resistor ratio $(R_2\|R_4)/(R_1'\|R_3')$ in (10) will increase as V_{out} approaches the supply rails. This will compensate the A_2 reduction, and extend the linear output range by minimizing the $A_{2,\text{cl}}$ reduction with V_{out} variation. Fig. 5(b) shows the linear output range extension under A_2 reduction, where the gains A_{ov} and A_2, and $(R_2\|R_4)/(R_1'\|R_3')$ with different V_{out} levels are obtained from nominal corner circuit simulation. The linear output range is considered as the amplifier output level with gain reduction less than 1.5 dB. As V_{out} varies from the midsupply level to the supply rails (V_{DD} or GND), the ratio $(R_2\|R_4)/(R_1'\|R_3')$ increases from 20 to 34 dB, where A_2 reduces from 30 to 7 dB. However, although A_{ov} degradation is mainly caused by A_2 reduction, A_1 reduction occurs when V_{out} is very close to the supply rails, which contributes to A_{ov} degradation as well. In this case, the linear output range is 3.05 V (0.1–3.15 V) with A_{ov} of 46.6 dB when V_{out} is at the midsupply (1.65 V).

To show the effect of first-stage pMOS and nMOS input pair mismatch and the resistors R_1–R_4 mismatch on A_{ov} and linear output range, Monte-Carlo simulations with 10% random mismatch between the pMOS and nMOS input pairs, and the second-stage resistors are performed. Fig. 6 shows the Monte-Carlo simulation results (200-runs) for (a) A_{ov} and (b) the linear output range. The distribution of A_{ov} is between 45 and 48.5 dB, where the gain does not significantly reduce with mismatch. The results show more than 60% of the occurrence is greater than 3 V (more than 90% of the occurrence is greater than 2.9 V), which indicates the proper operation of the amplifier under mismatch. Furthermore, since the first stage is an open-loop configuration, process, supply voltage, and temperature variation can affect the gain. Simulation results show A_{ov} of 46.9 dB for the typical corner that increases to 48.1 dB for the slow–slow corner and decreases to 45.7 dB for the fast–fast corner. With supply variation, A_{ov} remains consistent within supply range of 1.5–3.3 V, where the input pairs and the gain enhancement switches properly function. This implies the proposed amplifier can operate with more than 50% supply voltage reduction. For temperature variation from −40 °C to 125 °C, A_{ov} varies between 45.2 and 47.6 dB (nominal corner), where A_{ov} reduces as temperature increases. This is due to the reference current variation in the amplifier bias circuitry.

C. Frequency Response

The lower 3-dB frequency of the proposed amplifier can be set by the external high-pass filter that eliminates the electrode offset. In addition, the upper 3-dB frequency can be adjusted by adding additional feedforward capacitors that will form a low-pass filter response with the first-stage output resistance. This is preferred by placing a capacitor at the output node of the amplifier, since a huge capacitor is required to obtain a low cutoff frequency due to the low output resistance of the buffer. Fig. 7 shows the two additional feedforward capacitors C_{c1} and C_{c2} included between the first and second stages, where the capacitors are placed at the first-stage buffer input to obtain a lower cutoff frequency. In addition, the s-domain block diagram of the proposed amplifier is shown in Fig. 8. $H_{\text{hp}}(s)$ represents the high-pass filter with cutoff frequency and gain of $\omega_{\text{php}} = 1/(2C_{\text{ext}} \cdot R_{\text{ext}})$ and $A_{\text{hp}} = 2C_{\text{ext}} \cdot R_{\text{ext}}$. For the first stage, there are two poles at the output node of the nMOS and pMOS input pairs (the mirror poles are neglected, since they are at a higher frequency) and two right half plane (RHP) zeroes due to C_{c1} and C_{c2}, however, assuming the two poles and the two RHP zeroes are at the same location, the first stage can be represented by a single pole ω_{p1} and a single RHP zero ω_{z1}. The second-stage $H_2(s)$ can be represented by a single-pole ω_{p2}. The complete frequency transfer function of the amplifier is given by

$$H(s) = \frac{A_{\text{hp}} A_1 A_{2,\text{cl}} s \left(1 - \dfrac{s}{\omega_{z1}}\right)}{\left(1 + \dfrac{s}{\omega_{\text{php}}}\right)\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)}. \quad (12)$$

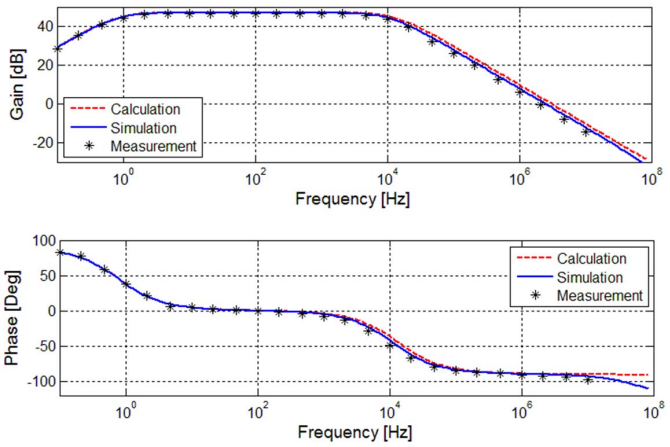

Fig. 9. Amplifier frequency response.

Assuming $C_c = C_{c1} = C_{c2}$, The first-stage pole can be obtained using Miller's theorem, which is given as

$$\omega_{p1} = \frac{1}{r_{o1}[c_{o1} + (1 + A_{2,\mathrm{cl}}) \cdot C_c]} \tag{13}$$

where r_{o1} and c_{o1} are the equivalent resistance and capacitance at the output node of the first stage. In addition, since the output resistance of the buffer R_{buff} is much less than the feedback resistors R_2 and R_4, the RHP zero due to the feedforward capacitor C_c can be approximated as

$$\omega_{z1} = \frac{A_2 \cdot R_{2,4}}{C_c R_{\mathrm{buff}} \cdot (R_{1,3} + R_{2,4})}. \tag{14}$$

However, ω_{z1} will be located at a much higher frequency compared with ω_{p1} and ω_{p2} due to the low R_{buff}. Furthermore, the second-stage pole is obtained by the load capacitance C_L and amplifier output resistance R_{out}. That is

$$\omega_{p2} = \frac{1}{R_{\mathrm{out}} C_L} \tag{15}$$

where assuming $R_{\mathrm{buff}} \ll R_{2,4}$, R_{out} is given by

$$R_{\mathrm{out}} = \frac{R_{\mathrm{buff}}}{1 + \dfrac{A_2 R_1}{(R_1 + R_2)} + \dfrac{A_2 R_3}{(R_3 + R_4)}}. \tag{16}$$

Fig. 9 shows the frequency response (magnitude and phase) of the proposed amplifier with $C_{\mathrm{ext}} = 0.22\ \mu$F, $R_{\mathrm{ext}} = 2$ MΩ, and $C_{c1} = C_{c2} = 0.5$ pF. The calculated frequency response is based on (12), and the simulation result is obtained from the amplifier transistor level circuit. However, the maximum frequency for the measured results only shows up to 10 MHz, which is due to the frequency limitation of the measurement setup. The frequency response of the proposed amplifier (up to 10 MHz) is mainly determined by ω_{php}, ω_{p1}, and ω_{p2}, where the effect of ω_{z1} is not significant. The discrepancy between the calculation and the simulation, measurement is the location of ω_{p1} and ω_{p2}, which are located at lower frequency for the simulation and measurement. This is expected to be due to additional parasitic capacitance. In addition, for the phase response, the phase shift near dc is due to the external high-pass filter, however, the pure phase shift of the proposed amplifier up to the unity gain frequency is around −90°, which leads to a sufficient phase margin.

Due to the off-chip components C_{ext} and R_{ext}, the input impedance of the proposed amplifier is 8.3–4.0 MΩ within the frequency range of 0.1 Hz–10 kHz. However, a higher input impedance can be obtained by scaling R_{ext} and C_{ext} so that the lower 3-dB frequency of the amplifier is not affected. With $C_{\mathrm{ext}} = 0.022\ \mu$F and $R_{\mathrm{ext}} = 20$ MΩ, the input impedance increases to 82.7–40 MΩ within the frequency range of 0.1 Hz–10 kHz.

III. Noise, CMRR, and PSRR Performance

A. Noise

Biopotential signals differ in magnitude from patient to patient. For ECG signals, the amplitude is typically in the range of 80 μV–5 mV [18]. With such small amplitudes, the quality of the acquired signals can be easily corrupted with noise, where the effect of $1/f$ noise will be significant due to the low frequency nature of biopotential signals.

For the proposed amplifier, since the first stage will mainly contribute to the input referred noise, noise reduction will be focused on the first-stage input pairs. Assuming an identical g_m for the nMOS and pMOS input pairs, and neglecting the second-stage noise, the input referred thermal noise power is given by

$$v_{\mathrm{ni,Th}}^2 = \left(\frac{8}{3}\mathrm{kT}\right) \cdot \left[\frac{1}{g_{m\mathrm{NP}}} + \frac{g_{m3,4}}{2g_{m\mathrm{NP}}^2} + \frac{g_{m5,6}}{2g_{m\mathrm{NP}}^2}\right] \cdot \Delta f \tag{17}$$

where $g_{m\mathrm{NP}} = g_{m1,2} = g_{m5,6}$, and the first-stage g_m is set to $2g_{m\mathrm{NP}}$ due to the complementary input devices. Again neglecting the second-stage noise, the input referred $1/f$ noise power can be written as

$$v_{\mathrm{ni},1/f}^2 = \left(\frac{1}{2C_{\mathrm{ox}} f}\right) \cdot \left[\frac{K_n}{W_n L_n} + \frac{K_p}{W_p L_p} + \frac{K_p L_p}{W_p L_{3,4}^2} + \frac{K_n L_n}{W_n L_{7,8}^2}\right] \cdot \Delta f \tag{18}$$

where K_n and K_p are the $1/f$ noise constants and W_n, L_n and W_p, L_p are the width and length of the nMOS and the pMOS input device, respectively. The general design procedure to minimize the input referred noise for biopotential amplifiers operating under extreme low power is to put the input-stage transistors in the weak inversion region [19], however, with low bias current levels, the g_m for the weak inversion will not be much different than the moderate inversion. And moreover, this will end up with a huge silicon area due to the large (W/L) ratio, $W \gg L$. As a result, for the proposed amplifier, the first-stage input devices (M_1, M_2 and M_5, M_6 shown in Fig. 2) operate in moderate inversion, however, due to the complementary input devices, the input referred noise will be reduced by a factor of $\sqrt{2}$ compared with the single device input pairs, since the g_m of the first stage is doubled. Furthermore, the first-stage active load transistors (M_3, M_4 and M_7, M_8) operate in strong inversion to reduce the noise contribution (the g_m of the active loads is set to approximately 1/10 of the input pairs). In addition, relatively large W and L

TABLE I
(a) NORMALIZED SENSITIVITY OF A_d AND ΔA_d WITH 10% MISMATCH OF $g_{m\mathrm{NP}}$, $R_{1,3}$, AND $R_{2,4}$. (b) NORMALIZED SENSITIVITY OF A_{cm} AND ΔA_{cm} WITH 10% MISMATCH OF $g_{m\mathrm{NP}}$, $R_{1,3}$, AND $R_{2,4}$

Normalized sensitivity	$\frac{\partial A_d}{\partial g_{mNP}} \cdot g_{mNP}$	$\frac{\partial A_d}{\partial R_{1,3}} \cdot R_{1,3}$	$\frac{\partial A_d}{\partial R_{2,4}} \cdot R_{2,4}$
Value	256.7	-423.0	-147.8
Mismatch	Δg_{mNP}	$\Delta R_{1,3}$	$\Delta R_{2,4}$
ΔA_d (in dB)	0.59	-1.85	-0.60

(a)

Normalized sensitivity	$\frac{\partial A_{cm}}{\partial g_{mNP}} \cdot g_{mNP}$	$\frac{\partial A_{cm}}{\partial R_{1,3}} \cdot R_{1,3}$	$\frac{\partial A_{cm}}{\partial R_{2,4}} \cdot R_{2,4}$
Value	1.5×10^{-2}	-2.6×10^{-2}	-9×10^{-3}
Mismatch	Δg_{mNP}	$\Delta R_{1,3}$	$\Delta R_{2,4}$
ΔA_{cm} (in dB)	1.21	-2.62	-0.82

(b)

values are used for the input devices to reduce the $1/f$ noise. With $(W/L)_{1,2} = (20/5\ \mu\mathrm{m})$ and $(W/L)_{5,6} = (60/5\ \mu\mathrm{m})$, and bias current of 0.7 μA, the simulated input referred noise is 5.07 $\mu\mathrm{V_{rms}}$. This is obtained by integrating the $1/f$ noise and thermal noise within the amplifier bandwidth of 0.7 Hz–10 kHz. The first stage contributes 98.5% of the total input referred noise, where the second-stage noise is negligible.

B. CMRR

CMRR degradation can add unwanted signal components at the output of the biopotential amplifier [20]. The CMRR of IA-based biopotential amplifiers is mainly affected by input-node impedance and feedback resistor mismatch. Moreover, the CMRR of CMIAs can be degraded by process induced transistor mismatch. The CMRR of the proposed amplifier is mainly determined by the first-stage differential pairs, where the CM gain of the nMOS and the pMOS differential pairs is given by

$$A_{\mathrm{cm},1n} \approx -\frac{g_{m1,2}}{(1+2g_{m1,2}\cdot R_{\mathrm{ssn}})g_{m3,4}} \tag{19a}$$

$$A_{\mathrm{cm},1p} \approx -\frac{g_{m5,6}}{(1+2g_{m5,6}\cdot R_{\mathrm{ssp}})g_{m7,8}} \tag{19b}$$

where R_{ssn} and R_{ssp} are the output resistance of the nMOS and pMOS differential pair tail current source, respectively. Furthermore, using (7), the overall CM gain can be written as

$$A_{\mathrm{cm}} = -\frac{\left(\frac{A_{\mathrm{cm},1n}}{R_1}+\frac{A_{\mathrm{cm},1p}}{R_3}\right)}{\frac{1}{(R_2||R_4)}+\frac{1}{A_2}\cdot\left[\frac{1}{(R_1\|R_2)}+\frac{1}{(R_3\|R_4)}\right]}. \tag{20}$$

Since the differential gain A_d (this is same as the overall gain A_{ov}) and the CM gain are affected by mismatch between the nMOS and the pMOS input pairs, R_1 and R_3, and R_2 and R_4, the mismatch effect on A_d and A_{cm} is investigated. Toward that end, the variation of A_d and A_{cm} with respect to the mismatches is described as

$$\Delta A_d = \left(\frac{\Delta g_{m\mathrm{NP}}}{g_{m\mathrm{NP}}}\right)\cdot\left(\frac{\partial A_d}{\partial g_{m\mathrm{NP}}}\cdot g_{m\mathrm{NP}}\right)+\left(\frac{\Delta R_{1,3}}{R_{1,3}}\right)\cdot\left(\frac{\partial A_d}{\partial R_{1,3}}\cdot R_{1,3}\right)+\left(\frac{\Delta R_{2,4}}{R_{2,4}}\right)\cdot\left(\frac{\partial A_d}{\partial R_{2,4}}\cdot R_{2.4}\right) \tag{21a}$$

$$\Delta A_{\mathrm{cm}} = \left(\frac{\Delta g_{m\mathrm{NP}}}{g_{m\mathrm{NP}}}\right)\cdot\left(\frac{\partial A_{\mathrm{cm}}}{\partial g_{m\mathrm{NP}}}\cdot g_{m\mathrm{NP}}\right)+\left(\frac{\Delta R_{1,3}}{R_{1,3}}\right)\cdot\left(\frac{\partial A_{\mathrm{cm}}}{\partial R_{1,3}}\cdot R_{1,3}\right)+\left(\frac{\Delta R_{2,4}}{R_{2,4}}\right)\cdot\left(\frac{\partial A_{\mathrm{cm}}}{\partial R_{2,4}}\cdot R_{2.4}\right) \tag{21b}$$

where $g_{m\mathrm{NP}}$, $R_{1,3}$, and $R_{2,4}$ are the nominal value of the nMOS and the pMOS input pair g_m, feedback resistors R_1, R_3 and R_2, R_4, and $\Delta g_{m\mathrm{NP}}$, $\Delta R_{1,3}$, and $\Delta R_{2,4}$ are the mismatches. In addition, the sensitivity of A_d and A_{cm} with respect to $g_{m\mathrm{NP}}$, $R_{1,3}$ and $R_{2,4}$ are obtained using (7) and (20), respectively. Table I-(a) shows the normalized sensitivity of A_d, and ΔA_d with 10% mismatch of $g_{m\mathrm{NP}}$, $R_{1,3}$, and $R_{2,4}$, and Table I-(b) shows the normalized sensitivity of A_{cm}, and ΔA_{cm} with 10% mismatch of $g_{m\mathrm{NP}}$, $R_{1,3}$, and $R_{2,4}$. ΔA_d and ΔA_{cm} values under mismatches are obtained by multiplying the normalized sensitivity with each % mismatch of $g_{m\mathrm{NP}}$, $R_{1,3}$, and $R_{2,4}$. The 10% mismatch is based on the worst case matching for the given process technology. Results show A_d and A_{cm} are most sensitive to mismatch between R_1 and R_3. As a result, considering the three source of mismatches, the worst-case variation of A_d and A_{cm} with $\pm10\%$ random mismatch is expected to be around 3 and 4.5 dB, respectively. Fig. 10 shows the Monte-Carlo simulation results (200-runs) for A_d and A_{cm} including random mismatch up to 10% for the first-stage input pairs and the feedback resistors R_1, R_3 and R_2, R_4. Results show A_d variation from 45.6 to 48.7 dB and A_{cm} variation from -42.4 to -37.2 dB. This is nearly consistent with the sensitivity analysis results. Furthermore CMRR obtained from the Monte-Carlo simulation is within the range of 84.1–88.3 dB. Considering the nominal CMRR of 86.5 dB, this leads to CMRR degradation of only 2.5 dB for 10% mismatch between the two input pairs and the feedback resistors.

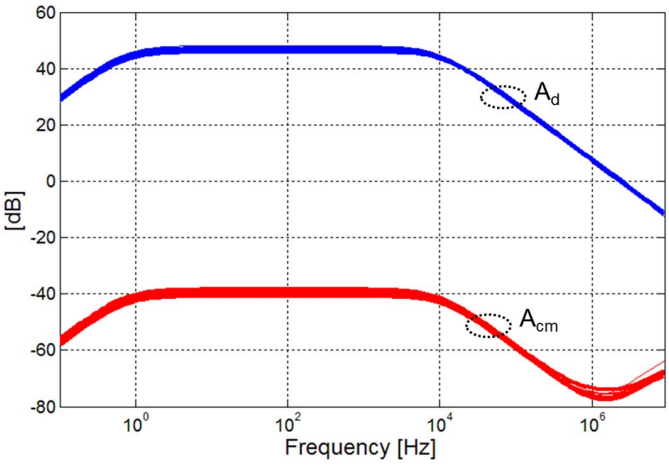

Fig. 10. Monte-Carlo simulation results for A_d and A_{cm}.

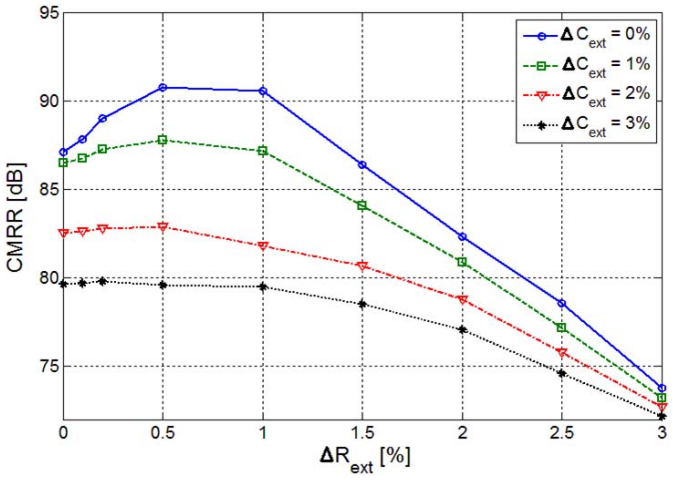

Fig. 11. CMRR at 100 Hz versus R_{ext} and C_{ext} mismatch (simulation).

The sensitivity analysis of A_d and A_{cm} is performed assuming perfect matching between the off-chip components C_{ext} and R_{ext}, however, mismatch caused by C_{ext} and R_{ext} leads to CMRR degradation. Fig. 11 shows the simulated CMRR at 100 Hz with C_{ext} and R_{ext} mismatch, where the mismatch is imposed between the positive and the negative input paths. Results show both C_{ext} and R_{ext} mismatch degrades the CMRR. However, without C_{ext} mismatch ($\Delta C_{\text{ext}} = 0\%$), the CMRR slightly increases for ΔR_{ext} around 1%, which is due to A_{cm} reduction. With both C_{ext} and R_{ext} mismatch of 2% and 3%, CMRR drops to 78.8 and 72.2 dB, respectively.

C. PSRR

Biopotential signals, such as the ECG and EEG are often contaminated by the 60-Hz power line interference. For ECG measurements, the CM spurs induced from the power line can be transformed into a differential error voltage due to unbalanced electrode-skin impedance [21]. Therefore, high PSRR is required for biopotential amplifiers to suppress the power line interference. However, since the positive power rail interference is more critical than the ground line interference, we will mainly investigate the positive supply rejection performance, PSRR+. The circuit model for positive supply power gain analysis is shown in Fig. 12. This includes three paths that connect the positive power supply V_{DD} to the amplifier output V_{out}. The signal path through the feedforward capacitors C_{c1} and C_{c2} are neglected, since this will have high impedance for low-frequency signals due to the small capacitance values. The overall power gain of the proposed amplifier is obtained by combing the gain of each path, which is given as

$$A_p = \frac{\left(1+\frac{R_2}{R_1}\right)}{1+\frac{1}{A_2}\left(\frac{R_2}{R_1}\right)} - \frac{\left(\frac{g_{mp}}{2g_{m7}}\right)\left(\frac{R_4}{R_3}\right)}{1+\frac{1}{A_2}\left(\frac{R_4}{R_3}\right)} - \frac{\left(\frac{R_2}{R_1}\right)}{1+\frac{1}{A_2}\left(\frac{R_2}{R_1}\right)} \tag{22}$$

where g_{mp} is the transconductance of M_p. As shown, the gain of path (i) is positive, whereas the gain of path (ii) and path

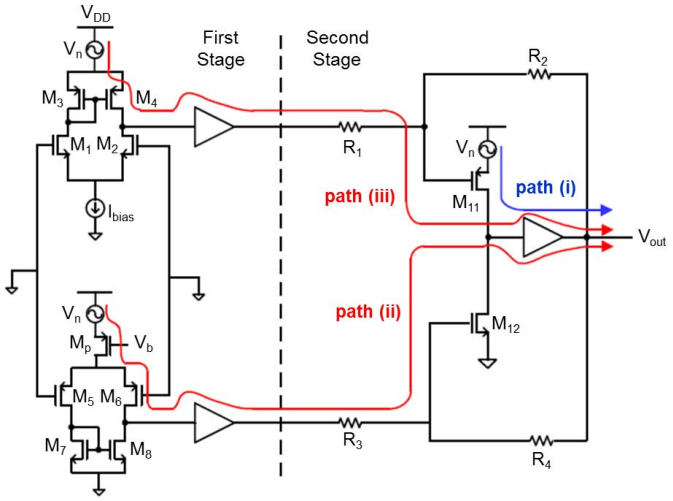

Fig. 12. Circuit model for PSRR+ analysis.

TABLE II
NORMALIZED SENSITIVITY AND ΔA_p WITH 10% VARIATION FOR R_1–R_4

Normalized sensitivity	$\frac{\partial A_p}{\partial R_1}\cdot R_1$	$\frac{\partial A_p}{\partial R_2}\cdot R_2$	$\frac{\partial A_p}{\partial R_3}\cdot R_3$	$\frac{\partial A_p}{\partial R_4}\cdot R_4$
Value	0.93×10^{-2}	-0.96×10^{-2}	0.12	-0.18
Variation	ΔR_1	ΔR_2	ΔR_3	ΔR_4
ΔA_p (in dB)	0.43	-0.54	1.24	-1.77

(iii) are negative. The power gain of the amplifier can be made nearly zero by setting ($g_{\text{mp}}/2g_{m7} = R_3/R_4$), which will significantly improve the PSRR+. The buffers can degrade the power gain of the amplifier, however, due to the negative feedback operation in the buffers, circuit simulation results show buffer power gain of −66 dB, which is negligible compared with the amplifier power gain.

The degradation of the power gain with respect to variation in the feedback resistors is investigated. However, in this case, since the paths from the supply noise input v_n to the amplifier output are not symmetric (as for the case of A_d and A_{cm}), instead of finding the sensitivity with mismatch between R_1–R_3 and R_2–R_4, the sensitivity of A_p for each resistor variation is considered. The degradation of A_p with respect to resistor variation is given as

$$\Delta A_p = \sum_{i=1}^{4}\left[\left(\frac{\Delta R_i}{R_i}\right)\cdot\left(\frac{\partial A_p}{\partial R_i}\cdot R_i\right)\right] \tag{23}$$

where ΔR_i, i = 1–4 is the variation of each resistor. Table II shows the normalized sensitivity of A_p, and ΔA_p with 10% resistor variation. Results show A_p of the proposed amplifier is more sensitive to R_3 and R_4 variation compared to R_1 and R_2 variation. In addition, the worst-case A_P degradation is expected to be around 4 dB with ±10% random variation in all the resistors. This implies the effect of resistor variation is somewhat nullified, since the (R_2/R_1) and the (R_4/R_3) terms are both included in the numerator and the denominator of A_p. The g_{mp} and g_{m7} variation will also affect A_p, however, this effect will be minor, since A_p is determined

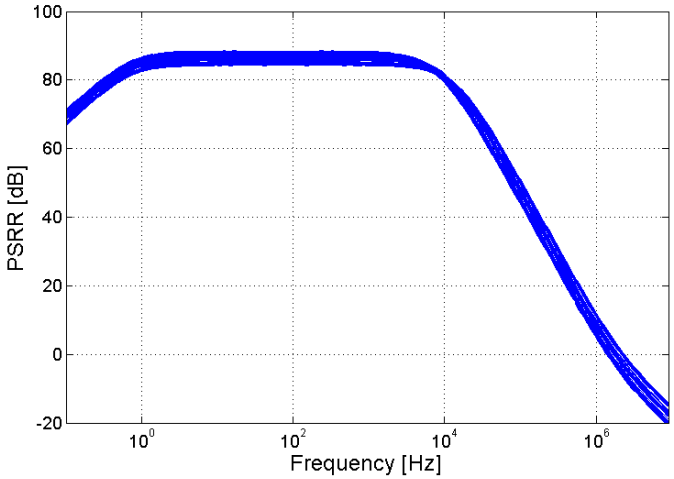

Fig. 13. Monte-Carlo simulation results for PSRR.

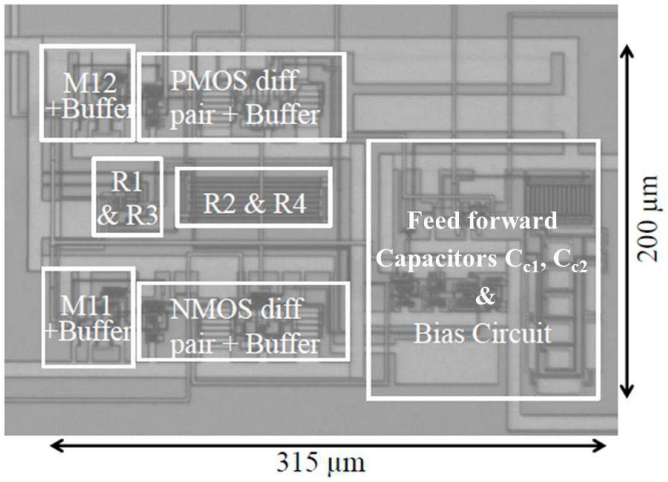

Fig. 15. Chip micrograph.

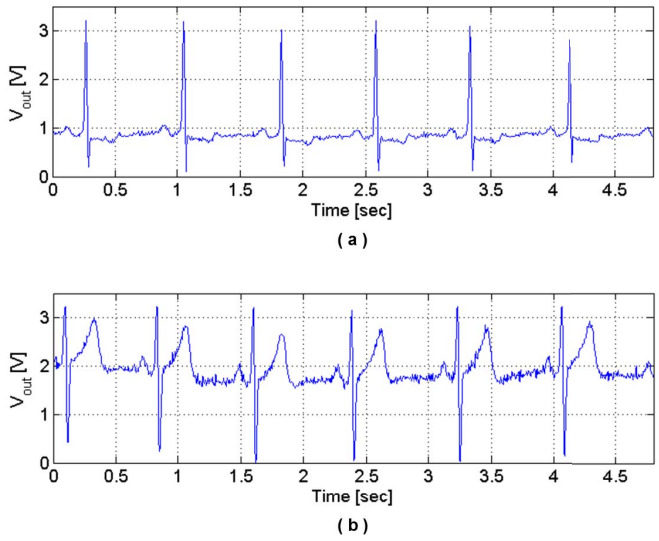

Fig. 14. Amplifier output waveform with MIT-BIH database ECG signals. (a) Record 105. (b) Record 219.

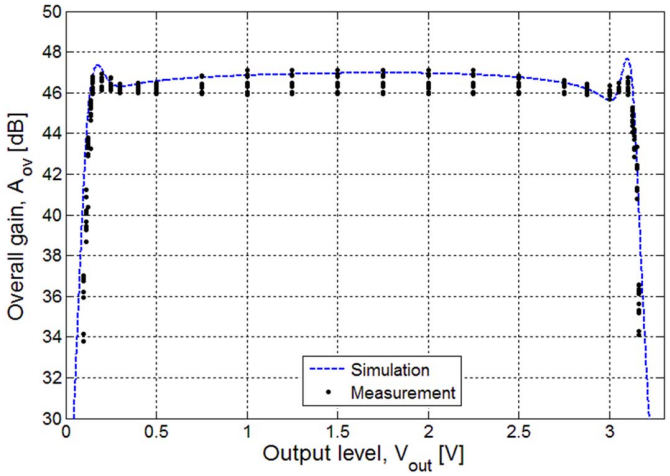

Fig. 16. Overall gain as a function of output range.

by the ratio between g_{mp} and g_{m7} that are both from the pMOS input pair. Fig. 13 shows the Monte-Carlo simulation results (200-runs) for PSRR with 10% random variation in all resistors R_1–R_4. The PSRR ranges from 83.7 to 88.4 dB, which is an acceptable value in case the biopotential measurement front is battery operated.

IV. Simulation Waveforms With ECG Database

Along with the basic electrical characteristics, the proposed amplifier is simulated using ECG signals. The two ECG signals used as the amplifier input are obtained from the MIT-BIH Arrhythmia database—Records 105 and 219 [22]. However, to show the amplifier output waveform within the full output range, the amplitude of the ECG input was adjusted for the simulation. In addition, to make the simulation setup similar to the human subject, an equivalent impedance of $R_{eq} = 500$ kΩ and $C_{eq} = 1$ μF obtained from the standard skin electrode interface is connected to the amplifier input node [23]. Fig. 14 shows the output waveform of the proposed amplifier with inputs (a) Record 105 and (b) Record 219. The output waveforms for both inputs do not show distortion, and the Q, R, S, and T waves are clearly shown.

V. Experimental Results

The proposed amplifier is implemented using CMOS 0.35-μm technology, where R_1–R_4 are n-well diffusion resistors, and C_{c1} and C_{c2} are poly-to-poly capacitors. Fig. 15 shows the chip micrograph of the proposed amplifier including the bias circuit that generates the reference current for each circuit block. The core area of the proposed amplifier is 0.063 mm^2. The measurement setup consists of the two-layer printed circuit board test board, dc power supplies, signal generator, source meter (Keithley 2612), and data acquisition unit (NI, DAQ USB-6361) for amplifier output waveform capture and processing.

Fig. 16 shows the overall gain as a function of amplifier output range, where the measurement results show the data obtained from 10 chips. For the measurement, A_{ov} ranges

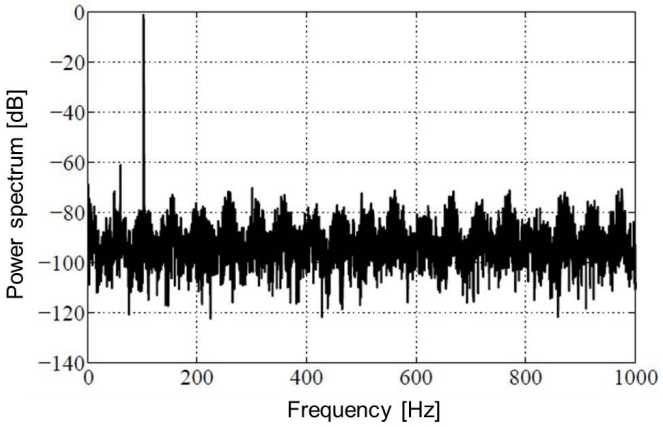

Fig. 17. Output spectrum with 100-Hz sine wave input.

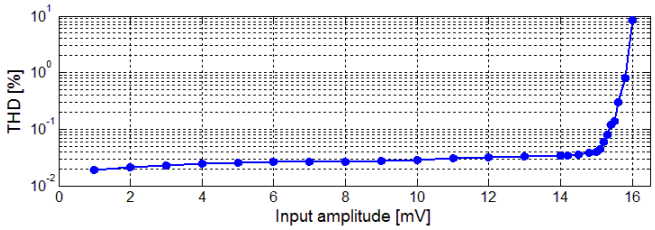

Fig. 18. THD versus input signal amplitude.

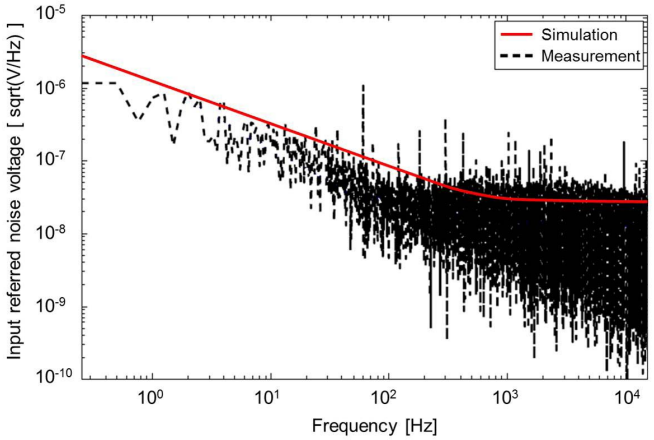

Fig. 19. Input referred noise spectrum.

from 45.9 to 47.1 dB with average of 46.3 dB. The linear output range of the amplifier is from 0.1 to 3.15 V for the simulation and from 0.15 to 3.12 V for the measurement, which leads to a linear output range of nearly 3 V. Fig. 17 shows the measured output spectrum with a 100 Hz (max. EEG signal frequency), 15 mV_{pp} sinusoidal input where the total harmonic distortion (THD) is 0.04%. The 15 mV_{pp} input covers the full linear output range of the amplifier. Fig. 18 shows the THD with input signal amplitude, where the input frequency is set to 100 Hz for all cases. It is shown that THD ranges from 0.019% to 0.04% with input amplitude from 1 to 15 mV_{pp}. THD degrades significantly for input amplitude greater than 15 mV_{pp}, where the output amplitude exceeds the linear output range of the amplifier. Fig. 19 shows

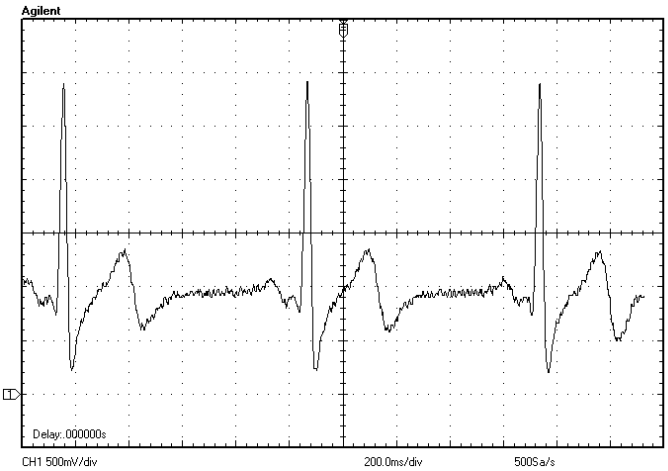

Fig. 20. Amplified ECG waveforms obtained from human subject (200 ms/div).

the measured input referred noise spectrum that is obtained by taking the fast Fourier transform of the time-domain noise waveform. In this case, the amplifier output is captured without applying the input signal, and divided by the overall gain to find the input-referred noise waveform. The noise spectrum shows thermal noise level of 34.63 nV/$\sqrt{\text{Hz}}$ with $1/f$ noise corner around 1.1 kHz. Fig. 20 shows the ECG waveform obtained from the actual human subject using commercial skin electrodes (Life Patch, Physio-Control Corporation). A two-electrode configuration is used with the external high-pass filter with $R_{\text{ext}} = 2$ MΩ and $C_{\text{ext}} = 0.22$ μF to eliminate the electrode offset. The amplified ECG signal is within the range of 0.2–2.95 V, which is in the linear output range. In addition, the amplified ECG signal clearly shows the Q, R, S, and T waves without distortion.

Table III shows the measured performance of the proposed amplifier compared with state-of-the-art biopotential amplifiers, where for the biopotential recording ICs [24], [28], [29], only the frontend amplifiers are considered. The voltage gain of the proposed amplifier is the average value obtained from 10 different parts. CMRR is measured with and without the off-chip components (C_{ext}, R_{ext}), where CMRR drops to 76.5 dB with the off-chip components. However, this can be improved by using higher tolerance off-chip components (less than 1%). The tolerance of C_{ext} and R_{ext} used in the CMRR measurement is ±5%. In addition, the input referred noise is obtained within the amplifier bandwidth of 0.7 Hz–10 kHz. The proposed amplifier shows slightly better CMRR and comparable PSRR compare with other amplifiers, except for [26] that has the highest CMRR among the other amplifiers. In addition, the THD (0.04% for input amplitude of 15 mV_{pp}) is better than other amplifiers, which is enabled by the wide linear output range. The input amplitude of 15 mV_{pp} is sufficient to accommodate various extracellular biopotential signals. Although the input referred noise of the proposed amplifier is slightly higher than the state-of-the-art amplifiers, the noise efficiency factor (NEF) is comparable with [24] and [26], which is a result of the power efficient design. Obviously the 3.3 V supply leads to a higher power con-

TABLE III
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART BIOPOTENTIAL AMPLIFIERS

Ref.	[24]	[25]	[26]	[27]	[28]	[29]	**This work**
Technology	CMOS 65nm	CMOS 0.13μm	CMOS 0.18μm	CMOS 0.13μm	CMOS 0.18μm	CMOS 0.18μm	**CMOS 0.35μm**
Gain (dB)	32	40	40 – 70	40	30 - 72	52	**46.3**
CMRR (dB)	75	80	120	78	60	73	**85.0**
PSRR (dB)	64	80	-	80	76	80	**83.2**
THD (%) @ Input amplitude	1% @ $0.2mV_{rms}$	1% @ $1mV_{pp}$	-	1% @ $16.5mV_{pp}$	1% @ $18mV_{pp}$	0.59% @ $2mV_{pp}$	**0.04% @ $15mV_{pp}$**
BW (kHz)	10	10.5	0.1	19.9	0.2	10	**10**
Input referred noise (μV_{rms})	4.9	2.2	0.88	3.7	3.2	3.2	**5.16**
NEF	5.3	2.9	4.7	3.04	2.72	1.57	**4.79**
Supply voltage (V)	0.5	1.0	0.4	1.5	1.8	0.45	**3.3**
Current (μA)	8.26	12.1	0.22	2.6	10.7	1.62	**5.6**
Power (μW)	4.13	12.1	0.09	3.9	10.48	0.73	**18.5**
Area (mm^2)	0.0037	0.072	0.28	0.03125	-	0.1*	**0.063**

*Estimated core area of single-channel LNA

sumption, however, due to the rail-to-rail input stage, proper operation is observed with reduced supply voltage (∼1.5 V). Furthermore, the proposed amplifier (even with the 0.35-μm technology) shows small area compared with [24], [26], and [29]. The small area is obtained by the compact amplifier architecture and efficient design optimization. The input offset of the proposed amplifier varied from 0.18 to 2.47 mV with average of 1.31 mV for 10 different chips. Dummy devices and common centroid layout techniques are applied for the nMOS and pMOS input pairs, and relatively large size devices—$(W \cdot L)$ of 100 μm^2 (nMOS) and 300 μm^2 (pMOS) are used to improve the matching and eventually reduce the input offset.

Overall, although the linear output range of the proposed amplifier can be effectively extended while achieving a reasonable CMRR and NEF, still several demerits of the design exist. First, the first-stage open-loop configuration can be more sensitive to mismatch for advanced CMOS technology. Second, the on-chip implementation of the external electrode offset cancellation circuitry can increase the core area, and finally, an additional amplifier input offset cancellation scheme can be required for extremely low amplitude biopotential acquisition.

VI. CONCLUSION

In this paper, we propose a wide linear output range biopotential amplifier for physiological measurement frontend. The wide linear output range is achieved by effectively combining the first-stage open-loop and the second-stage closed-loop configuration, and using additional gain enhancement switches. Due to the wide linear output range, the proposed amplifier shows a stable voltage gain of 46.3 dB for output range from 0.15 to 3.12 V and THD of 0.04% with a 15 mV_{pp} input amplitude (all with 3.3 V supply). In addition, the voltage gain and linear output range of the proposed amplifier do not significantly change with different process corners, and the CMRR and PSRR are not sensitive to feedback resistor mismatch. Furthermore, both the simulation and measurement results demonstrate the proper operation of amplifier with actual physiological signals. Overall, with a signal bandwidth of 10 kHz, the proposed amplifier is suitable for ECG, EEG, and electromyogram measurement frontends, where the dynamic range will be extended by maximizing the input range of the ADC. However, although the proposed amplifier is realized with a CMOS technology with supply voltage of 3.3 V, it can be simply adopted to advanced CMOS technologies with lower supply voltages.

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