

A Triple-Loop Inductive Power Transmission System for Biomedical Applications

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Abstract—A triple-loop wireless power transmission (WPT) system equipped with closed-loop global power control, adaptive transmitter (Tx) resonance compensation (TRC), and automatic receiver (Rx) resonance tuning (ART) is presented. This system not only opposes coupling and load variations but also compensates for changes in the environment surrounding the inductive link to enhance power transfer efficiency (PTE) in applications such as implantable medical devices (IMDs). The Tx was built around a commercial off-the-shelf (COTS) radio-frequency identification (RFID) reader, operating at 13.56 MHz. A local Tx loop finds the optimal capacitance in parallel with the Tx coil by adjusting a varactor. A global power control loop maintains the received power at a desired level in the presence of changes in coupling distance, coil misalignments, and loading. Moreover, a local Rx loop is implemented inside a power management integrated circuit (PMIC) to avoid PTE degradation due to the Rx coil surrounding environment and process variations. The PMIC was fabricated in a 0.35- μm 4M2P standard CMOS process with 2.54 mm² active area. Measurement results show that the proposed triple-loop system improves the overall PTE by up to 10.5% and 4.7% compared to a similar open- and single closed-loop system, respectively, at nominal coil distance of 2 cm. The added TRC and ART loops contribute 2.3% and 1.4% to the overall PTE of 13.5%, respectively. This is the first WPT system to include three loops to dynamically compensate for environment and circuit variations and improve the overall power efficiency all the way from the driver output in Tx to the load in Rx.

Index Terms—Adaptive resonance tuning, closed-loop wireless power transmission (WPT), implantable medical devices, radio-frequency identification (RFID), triple-loop power control.

I. INTRODUCTION

INDUCTIVE power transfer is used in many implantable medical devices (IMDs) to enhance their performance by increasing the number of electrodes, stimulation current, and stimulus rate [1]–[6]. Compared to batteries or transcutaneous interconnects, inductive powering is safer, more convenient for the patient, and smaller in size. Inductive links have also been used in near-field radio-frequency identification (RFID)

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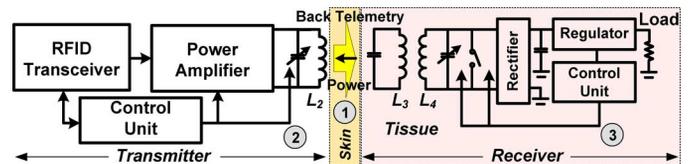


Fig. 1. Triple-loop inductive wireless power transmission using a 3-coil link.

to power up and interrogate transponders [7]. More recently, inductive links have also gained attention in charging mobile electronics and electric vehicles [8]–[13]. The transmitter (Tx) in an inductively-powered system includes a power amplifier (PA) followed by a matching circuit and the primary coil, L_2 , as shown in Fig. 1. In a 3-coil configuration, the receiver (Rx) includes two coils, L_3 and L_4 , in which L_4 is used for impedance matching with the load, followed by a power management circuitry for voltage rectification and regulation [14]–[16].

In IMDs, high power transfer efficiency (PTE) is desired to reduce heat dissipation in the coils, exposure to electromagnetic field (which can cause additional heat dissipation in the medium), size of the external energy source (e.g., battery), and interference with nearby electronics that is necessary to satisfy regulatory requirements [17]–[19]. Hence, over the last decades several methods have been proposed to enhance the PTE, such as geometrical optimization of the 2-, 3-, and 4-coil inductive links [14]–[16], [20]–[28]. However, in practice, optimizing the coil geometries alone is not sufficient to maintain high PTE.

In addition to the geometry and alignment, the PTE is highly dependent on how well the Tx and Rx tank circuits are tuned at the operating frequency, f_p [29]. In IMDs, the inductive link is often adversely affected by the parasitic capacitance of the surrounding tissue environment, which can significantly degrade the PTE, particularly when the Q-factor is high [21]. A few methods have been proposed to adaptively tune the Rx LC-tank [30], [31]. These methods employ a variable LC-tank on the Rx side to compensate for variations in the Rx resonance capacitance. However, the Tx LC-tank detuning could still degrade the wireless link PTE. In particular, if the Tx coil happens to be planar and flexible to better conform to the outer body profile, both L_2 and parasitic components of C_2 in Fig. 1 could continuously change on the Tx side with body motion. To address this issue, an adaptive Tx that adjusts either the carrier frequency or the matching circuit of the Tx coil can be used. The adaptive f_p that tends to overcome the PTE degradation in real-time has been demonstrated in [32]–[34]. However, it could be inefficient when LC matching network with high Q-factor or frequency-sensitive PA topologies, such as class-E, have been

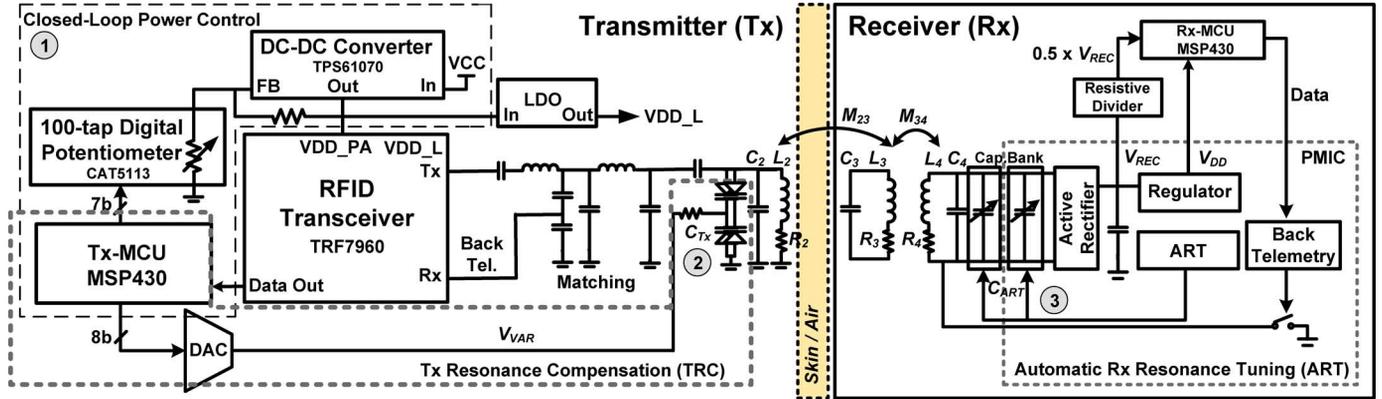


Fig. 2. Block diagram of the triple-loop power transmission system. An RFID reader on the Tx side drives the primary coil, L_2 , at $f_p = 13.56$ MHz and recovers the LSK back telemetry data from the Rx. On the Tx side, first control loop adjusts the power amplifier supply (V_{DD_PA}) to oppose coils' coupling and Rx loading variations. A second control loop (TRC) tunes the Tx LC-tank to compensate for any detuning due to environmental or physical changes to L_2 . On the Rx side, a high efficiency power management IC (PMIC) rectifies the AC carrier and a third loop (ART) automatically tunes the Rx LC-tank at f_p . A low power MCU digitizes $V_{REC}/2$ and sends the data serially to the PMIC to be keyed back to the RFID reader. This info is used for both closed-loop power control and Tx LC-tank tuning.

used. Moreover, compliance with regulations could be more complicated with a variable f_p and a simple Rx may not be able to continuously track the f_p variations.

Closed-loop power control is also required for efficient power transfer in the presence of coil coupling and loading variations [35]–[37]. Here, either the PA output power or f_p is adaptively adjusted to maintain the Rx voltage constant in the presence of perturbations. Although each control loop and a combination of two loops have been implemented and discussed in the literature ([30], [31], and [38]), a complete system with all three loops working together in real-time to address all the aforementioned issues has not been demonstrated.

In this paper, we demonstrate a triple-loop wireless power transmission system that includes 1) closed-loop power control, 2) adaptive Tx resonance compensation (TRC), and 3) automatic Rx resonance tuning (ART). The proposed system keeps the PTE of the wireless power transmission system dynamically at its peak by simultaneously operating these three loops, while maintaining the system robustness and stability. The Tx is built around a commercial off-the-shelf (COTS) RFID reader, operating at $f_p = 13.56$ MHz. To reduce size and power consumption, we have designed an application-specific power management integrated circuit (PMIC) for the Rx, which uses load-shift keying (LSK) for back telemetry [39]. In Section II, the three control loops are introduced. The control algorithm and stability analysis are presented in Section III. The PMIC ASIC is described in Section IV, followed by measurement results and conclusions in Sections V and VI, respectively.

II. SYSTEM ARCHITECTURE

Fig. 2 shows a simplified block diagram of the proposed triple-loop wireless power transmission system. In this system, a 13.56 MHz RFID reader (TRF7960) on the Tx side drives L_2 and recovers back telemetry data from the Rx. Independent loops in Tx adjust the LC-tank resonance capacitance (C_{Tx}) and PA supply voltage (V_{DD_PA}) to compensate for any environmental or physical (e.g., L_2 deformation) detuning and coupling/loading variations, respectively. On the Rx side, the PMIC ASIC rectifies and regulates the 13.56 MHz power

carrier and tunes the Rx LC-tank at the operation frequency, f_p . The rectifier voltage, V_{REC} , is divided in half and digitized in 10 bits by an MSP430 microcontroller, which combines them with start bits, “01”, following a 300 μ s-long stream of zeroes, and sends them back to the Tx through the PMIC ASIC by shorting L_4 at a rate of 250 kHz. V_{REC} information on the Tx side is then used by both the TRC and power control loops.

A. Automatic Resonance Tuning

The ART is implemented locally in the PMIC ASIC using a combination of internal and external switched-capacitor banks. The 13.56 MHz carrier is rectified by a high efficiency full-wave active rectifier, followed by a low dropout (LDO) regulator to provide $V_{DD} = 3.3$ V for the rest of the system [40].

The ART seeks maximum PTE in the presence of any undesired varying parasitic capacitance, C_{PAR} , imposed by the Rx surrounding environment (e.g., human body), by tuning L_4 at $f_p = 13.56$ MHz. In the ART block, two 5-bit binary-scaled on-chip and off-chip capacitor banks are swept within $L_4 C_4$ -tank. The envelope of the carrier signal across $L_4 C_4$ -tank is sampled before and after stepping C_{ART} to decide the direction of the total capacitance change in real-time. We have added a small base capacitance, C_4 , in parallel with L_4 for proper startup when the ART loop is off or disabled. The ART ensures that $(C_4 + C_{ART} + C_{PAR})$ perfectly resonates with L_4 at f_p .

B. Closed-Loop Power Control

The RFID reader not only drives L_2 by its built-in class-D PA but also recovers the LSK back telemetry signal, which is over-sampled by the Tx MCU (MSP430). V_{REC} data is then used to adjust the V_{DD_PA} inside the RFID reader. In this prototype, V_{DD_PA} is generated by a high efficiency DC-DC converter (TPS61070), and it is adjustable from 3 V to 5.5 V in 100 steps through a digital potentiometer (CAT5113). The Tx MCU continuously searches for a 300 μ s zero bit stream followed by the start bits “01”. When “01” bits are detected, it recovers the rest of the 10-bit packet, which is V_{REC} . Considering the efficiency and dropout voltage of the LDO, the upper

and lower threshold voltages are designated at 4.2 V and 3.6 V, respectively. To maintain V_{REC} inside a designated range of lower $V_{RLT} = 3.6$ V and upper $V_{RUT} = 4.2$ V thresholds, the binary value of $V_{REC}/2$ is compared with a programmable window (650 ~ 560) in the MCU. If $V_{REC} < V_{RLT}$, the MCU increases the V_{DD_PA} and vice versa. If V_{REC} is inside the desired window, V_{DD_PA} is not changed. In the presence of any external disturbance, the Tx MCU reduces or increases the transmitted power until it receives a value within 560–650 [36].

C. Transmitter Resonance Compensation

Although the Tx LC-tank can be manually tuned before its operation, in most applications, including IMDs, the resonance conditions constantly change during the operation when the Tx coil is exposed to variable surrounding environments or bends as a result of body movements. Therefore, an adaptive Tx LC-tank resonance compensation (TRC) circuit can improve the PTE. Based on our previous measurements in [21], parasitic capacitance variations for printed spiral coils (PSCs) with 2.4 cm in diameter can be up to 7.72 pF in the muscle environment.

The prototype TRC (Fig. 2) was composed of an MCU, an 8-bit digital-to-analog converter (DAC) (Max 522), and four varactors (SMV 1265). The MCU controls the DAC output voltage, V_{VAR} , and the total capacitance of the varactors, C_{Tx} , changes from 22.47 pF to 6.1 pF by changing V_{VAR} from 0 to 3.3 V. Anti-series configuration for varactors is utilized to achieve lower distortion than a single varactor connection [41]. The TRC loop changes V_{VAR} and the L_2C_2 -tank resonance to achieve maximum V_{REC} for any particular V_{DD_PA} value, which corresponds to the peak resonance condition on the Tx side.

III. TRIPLE-LOOP CONTROL ALGORITHM

Fig. 3 shows the flowchart of the triple-loop control algorithm that maintains the rectifier voltage, V_{REC} , within a designated range in response to different types of external disturbances to the wireless power transmission (WPT) link, while ensuring its high PTE and stability. In order to maintain simplicity of the system and low power consumption, we have avoided a central controller that would observe simultaneous operation of the three loops, which would have required a separate wireless data communication path. Instead, the control algorithm sequentially activates one loop at a time, normally in this order: 1) power, 2) TRC, and 3) ART, at the cost of a somewhat slower response time.

During start-up, the Tx MCU sets the DC-DC converter output to $V_{DD_PA} = 3$ V, which corresponds to the lowest RF power. It gradually increases the V_{DD_PA} until enough power is delivered to the PMIC to enable the back telemetry link. The RFID reader detects the LSK pulses and the global power control loop becomes operational. This loop has the highest priority in the system to ensure that Rx receives the minimum required power to remain operational. The programmable window ($V_{RUT} - V_{RLT}$) for V_{REC} limits fluctuations due to noise or instability. If the received V_{REC} through back telemetry is outside this window, the power loop adjusts V_{DD_PA} in proper direction until V_{REC} returns inside the desired range.

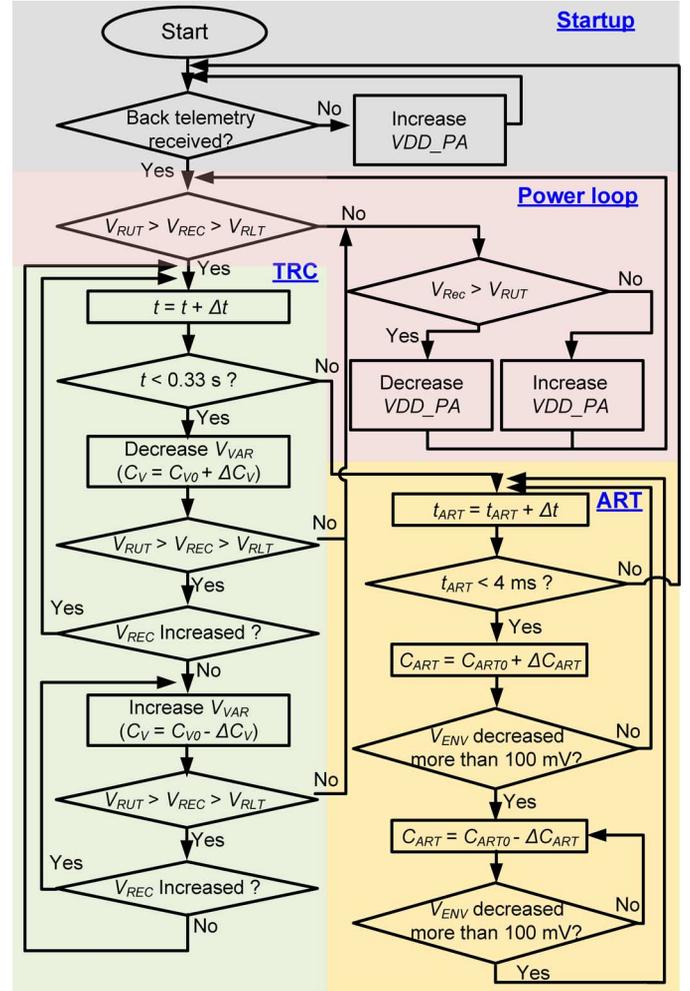


Fig. 3. Flow chart of the triple-loop wireless power transfer control algorithm.

Once V_{REC} is within $V_{RUT} - V_{RLT}$, the power loop is disabled and TRC loop is enabled to find the optimal resonant capacitance for the L_2C_2 -tank. The control algorithm in the Tx MCU increases V_{VAR} to decrease C_{Tx} in Fig. 2 until V_{REC} starts decreasing. Then it decreases V_{VAR} and monitors V_{REC} until C_{Tx} passes the optimal resonance value, at which point V_{REC} starts decreasing again, and the MCU switches the direction of V_{VAR} variations. This up/down cycle ensures that C_{Tx} wiggles around its optimal value, while responding to the environmental inputs. Considering 256 steps in the 8-bit DAC and the varactor used in this prototype (SMV 1265), there is a 70 fF capacitance change across the L_2C_2 -tank for every step. The high resolution varactor-based TRC design prevents sudden voltage variations across L_2 without adding the bulk of an 8-bit capacitor bank.

If V_{REC} exits $V_{RUT} - V_{RLT}$ window during TRC operation, the TRC loop is immediately paused and the power loop is enabled to return V_{REC} back to the designated range. The TRC loop is then activated again to tune C_{Tx} at the new PA output power. The TRC loop may also time-out after 0.33 s by the Rx MCU internal timer, which activates the ART loop to fine-tune C_{ART} on the Rx side.

The ART loop operates based on a 26 kHz clock, extracted in the PMIC from the 13.56 MHz power carrier. A 10-bit capacitor

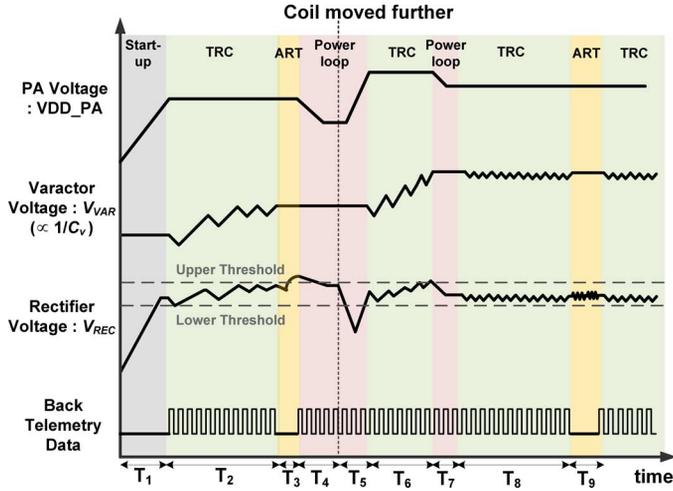


Fig. 4. Conceptual transient waveform for the triple-loop control algorithm operation in response to a disturbance (reduction) in the coils' coupling.

bank, C_{ART} , is swept across L_4C_4 -tank in both directions (up/down) to fine tune the L_4C_4 -tank every 0.33 s by maximizing the received power carrier envelope (V_{ENV}). In steady state, V_{ENV} reaches its maximum level and wiggles around it with a 100 mV ripple. The ART loop finds the optimal C_{ART} in less than 3 ms if it only utilizes the 5-bit on-chip capacitors. Details of the ART control loop have been included in Section IV along with the details of the PMIC ASIC. Since the ART loop operates much faster than the TRC and power control loops, it is enabled only for ~ 4 ms every 0.33 s. Back telemetry is disabled during the ART operation to prevent erroneous RFID readings on the Tx side.

Fig. 4 shows an exemplar operation of the sequential control algorithm in Fig. 3 and the resulting key transient waveforms. During T_1 start-up period, PA output power increases until V_{REC} is enough to initiate back telemetry data. Once V_{REC} reaches the designated window, shown with horizontal dashed lines, the power loop is deactivated and the TRC loop starts to adjust C_{VAR} to find max V_{REC} for the given PA output power at the end of T_1 . The ART loop starts after $T_2 = 0.33$ s is timed-out and continues periodically for $T_3 = 4$ ms, while back telemetry is disabled. During T_3 , V_{REC} is increased by the ART loop while the Rx L_4C_4 -tank is fine-tuned and may exceed the upper threshold, as shown in Fig. 4. If this occurs, during T_4 the power control loop decreases the PA output power to return V_{REC} back to the designated range, $V_{RUT} - V_{RLT}$.

If there is a sudden change in the coils' coupling, e.g., k_{23} reduction in Fig. 2, or a sudden increment in the Rx power consumption at the end of T_4 , which is identified by a vertical dashed line in Fig. 4, V_{REC} will drop below V_{RLT} and the power loop immediately reacts by increasing VDD_PA during T_5 . During T_6 , the TRC loop pushes V_{REC} beyond the upper threshold, which results the power loop activation during T_7 to reduce the PA output power. Following the same routine, the TRC and ART loops alternate during T_8 , T_9 , and beyond, respectively, to maximize the PTE, keep V_{REC} within $V_{RUT} - V_{RLT}$, and tune the Tx and Rx resonant tanks at f_p .

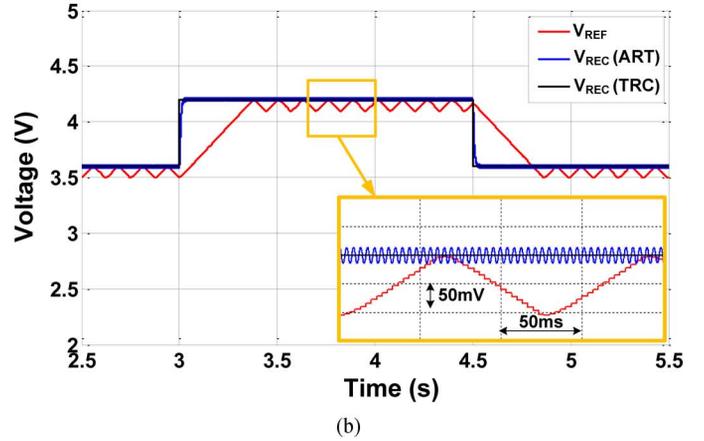
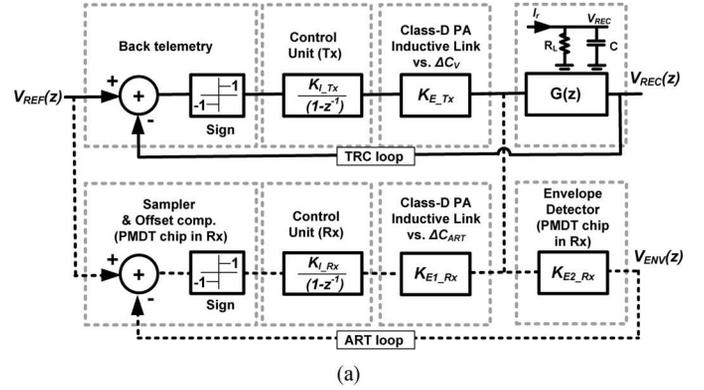


Fig. 5. (a) Discrete-time model of the TRC and ART loops in the triple-loop wireless power transmission system. (b) Simulated transient step response of the TRC and ART loops in Simulink.

According to the control algorithm in Fig. 3, the three loops operate at different time periods to maintain the triple-loop system stability as long as each individual loop is stable. The requirements for the stability of the global power loop have already been studied and presented in our previous work [36]. In this implementation, we have chosen the power update frequency to be 300 Hz, resulting in a settling time of 500 ms.

The discrete-time model of the TRC and ART loops is shown in Fig. 5(a). The TRC loop is divided into four key building blocks; 1) back telemetry (BT) circuit, 2) control unit including the DAC, 3) the RFID class-D PA and inductive link, and 4) the resistive-capacitive (R_{LC}) load following the rectifier circuit in the Rx. The desired reference voltage, V_{REF} , is the system input and the Rx rectifier voltage, V_{REC} , is the system output. The BT circuit is modeled by an adder followed by a sign block, which compares V_{REC} and V_{REF} to generate an increment “+1” or decrement “-1” command for the class-D PA output power. A sampler with a comparator, which is designed to have a 100 mV offset as discussed in Section VI, constitutes the sign block.

The control units for the TRC and ART loops are modeled by the integrators with gains K_{I_Tx} and K_{I_Rx} , respectively. In the TRC loop, the control unit either increases or decreases the varactor voltage, V_{VAR} , using the Tx DAC, based on the BT data. Therefore, K_{I_Tx} is determined by the capacitance variation of the varactor, ΔC_V , for a least significant bit (LSB) change in the DAC output. In the ART loop, the resolution of the capacitor bank across L_4C_4 -tank determines K_{I_Rx} . The

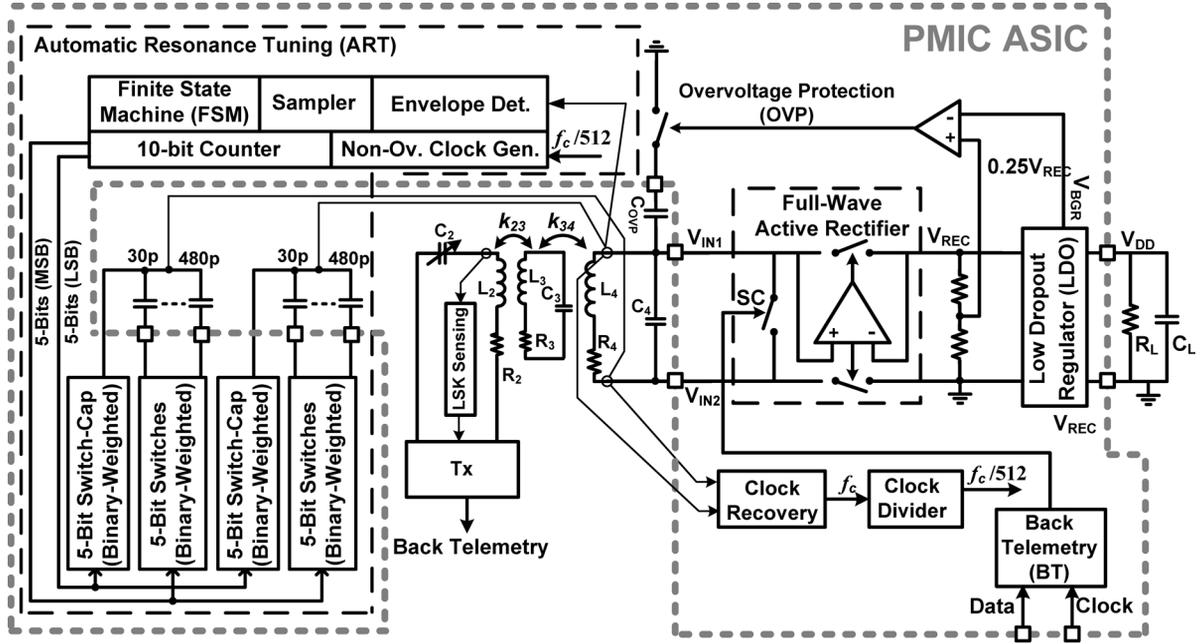


Fig. 6. Block diagram of the efficient and adaptive PMIC ASIC, developed specifically for inductively-powered devices operating at 13.56 MHz. The AC carrier is rectified by a full-wave active rectifier followed by an LDO to provide a constant 3.3 V supply. The ART block sweeps 0–480 pF across L_4C_4 -tank with 0.5 pF resolution to find the optimal capacitance to resonate with L_4 at 13.56 MHz in the presence of varying parasitic capacitance.

gain factors, K_{E-Tx} and K_{E1-Rx} , are determined by the ratio of the average current variation delivered to the RC load (ΔI_r) caused by a change in V_{DD_PA} , following ΔC_V and ΔC_{ART} changes in the TRC and ART loops, respectively. The TRC loop tracks V_{REC} via the BT circuit. In the ART loop, the sampler tracks the envelope voltage across L_4C_4 -tank, V_{ENV} , through an envelope detector and resistive divider in the PMIC ASIC, which are modeled by another gain factor, K_{E2-Rx} .

The capacitive and resistive components of the rectifier load current, $I_c[n]$ and $I_{RL}[n]$, are given by

$$I_c[n] = \frac{q[n] - q[n-1]}{T} = \frac{C(V_{REC}[n] - V_{REC}[n-1])}{T}$$

$$I_{RL}[n] = \frac{V_{REC}[n]}{R_L} \quad (1)$$

where T is the loop sampling period, which has significantly different values in the TRC ($T_{TRC} = 3.3$ ms) and ART ($T_{ART} = 77$ μ s) loops, depending on the controller time base and other component values. $V_{REC}[n]$ is the rectifier voltage at time $t = nT$, and q is the total charge stored in the rectifier capacitor. The impedance of the rectifier RC load, $G(z)$, in the z domain can be defined as

$$G(z) = \frac{V_{REC}(z)}{I_r(z)} = \frac{R_L}{1 + \frac{R_L C}{T} - \frac{R_L C}{T} z^{-1}}. \quad (2)$$

Since the discrete-time model for the TRC and ART loops is non-linear due to the presence of sign and offset comparator blocks, the system response was verified using Simulink (MathWorks, Natick, MA). The transient step responses of these loops to V_{REF} variation from $V_{RLT} = 3.6$ V to $V_{RUT} = 4.2$ V are shown in Fig. 5(b). When V_{REC} is out of this window,

the power loop regulates V_{REC} to return within these boundaries. It can be seen that each loop follows the step response and fluctuates within a narrow voltage range. In the TRC loop, the 103 mV fluctuation is defined by the resolution of the ADC and DAC in the Rx MCU and TRC loop, respectively. In the ART loop, the 28 mV fluctuation depends on the comparator offset in the PMIC ASIC. T_{TRC} and T_{ART} also affect the settling time and voltage range. When T_{TRC} and T_{ART} decrease, the voltage fluctuations and settling time also decrease. The settling times of the TRC and ART loops for the above step response, were 360 ms and 20 ms, respectively. These are the maximum settling times for the worst-case disturbance of the TRC and ART loops.

IV. POWER MANAGEMENT ASIC

Fig. 6 shows the block diagram of the PMIC ASIC, which includes an active rectifier, a 3.3 V low dropout (LDO) regulator, the ART circuitry, and the LSK circuitry for back telemetry. The ART sweeps two 5-bit binary-weighted on-chip (1 pF, 2 pF, 4 pF, 8 pF, 16 pF) and off-chip (30 pF, 60 pF, 120 pF, 240 pF, 480 pF) capacitor banks resulting in a wide (0–480 pF) capacitance tuning change across L_4 with 0.5 pF resolution. There is also an over-voltage protection (OVP) hysteresis comparator that detunes the L_4C_4 -tank by the off-chip $C_{ovp} = 100$ nF when $V_{REC} > 4.8$ V to protect the PMIC input when the coupling is too strong or the loading is light (large R_L).

A. Full-Wave Active Rectifier

Fig. 7 shows a simplified schematic diagram of the PMIC active rectifier, consisting of PMOS and NMOS pass transistors, which are driven by two high-speed offset-controlled comparators to operate at 13.56 MHz [40]. The start-up circuit monitors V_{REC} and sets $CTL = 0$ when V_{REC} is low. Hence, P_1 and P_2

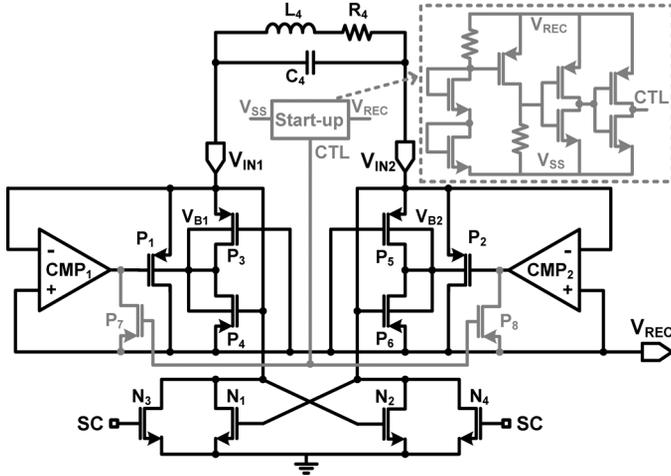


Fig. 7. Schematic diagram for full-wave active rectifier [40].

are diode-connected and form a passive rectifier, which charges V_{REC} regardless of the comparators' status until V_{REC} reaches a stable minimum level (1.6 V). Then CTL toggles to enable the active rectifier to operate normally.

B. Automatic Resonant Tuning and Back Telemetry

The ART sweeps two identical 10-bit capacitor banks, which are connected to a 10-bit counter, in one direction (up or down) until the voltage envelope across L_4C_4 -tank, V_{ENV} , reduces by 100 mV, as shown in Fig. 8. Then the sweeping direction changes until V_{ENV} again drops by 100 mV. This up/down cycle ensures that the L_4C_4 -tank is always tuned at $f_p = 13.56$ MHz with a small offset. V_{ENV} is first detected by a passive rectifier, divided by 1.4, and buffered before being sampled. Two non-overlapping clocks, CLK_C and CLK_S , are generated from the $f_p/512 = 26.4$ kHz signal that results from the clock recovery and divider blocks in Fig. 6. The first sampler, S_1 , always samples V_{ENV} at the rising edge of CLK_S while S_2 only samples V_{ENV} at the rising edge of CLK_C when V_{ENV} increases or decreases by 100 mV. $CMP_{1,2}$, which are 100 mV offset comparators, close S_3 when the difference between C_1 and C_2 voltages is ± 100 mV. When the offset voltage of the comparator decreases, the fluctuation voltage reduces. However, the system becomes more sensitive to external perturbations.

When V_{ENV} drops by 100 mV, CMP_2 output, which is labeled Dir_Ch in Fig. 8, changes the direction of the counter according to a finite state machine (FSM). The FSM starts the counter from the middle of the capacitor banks, 240 pF across the L_4C_4 -tank, when the PMIC is powered up. The counter operates at the falling edge of CLK_C to be time-shifted from V_{ENV} samplings at the rising edges. The back telemetry circuit creates ~ 250 ns pulses, when data is "1" to short the L_4C_4 -tank by closing the SC switches in the rectifier. An RC delay cell is used to generate the 250 ns delay. The data and clock signals are generated by the Rx-MCU, as shown in Fig. 2.

V. MEASUREMENT RESULTS

Fig. 9 shows the measurement setup of the proposed triple-loop system and the PMIC die photo. The PMIC ASIC was fab-

ricated in the TSMC 0.35- μm 4M2P standard CMOS process, occupying 2.54 mm² of silicon area. Printed spiral coils (PSC) were used for the primary (L_2) and load (L_4) coils, while a high-Q wire-wound coil (WWC) was used for the secondary coil (L_3) to maximize the 3-coil link PTE. The 3-coil link was designed based on the optimization procedure in [14] with the link specifications summarized in Table I. The maximum output power of the RFID reader is 200 mW, which was enough to transfer ~ 10 mW to the Rx at $d_{23} = 2$ cm nominal coupling distance. In this prototype, we chose a 3-coil link to perform impedance modulation on the Rx using an extra coil. Because we are using a class-D power amplifier with its LC-network matching circuit, there is no need for an additional coil on the Tx side [14].

Fig. 10(a) shows the steady state measured V_{REC} and counter direction flag (Dir_Ch) in the ART loop. Dir_Ch is periodically set high when V_{REC} drops by 0.3 V, indicating detuning from $f_p = 13.56$ MHz. This event changes the direction of the counter in Fig. 8 as well as the amount of added capacitance to C_4 in Fig. 6 (up to ~ 16 pF). V_{REC} peaks between two consecutive $Dir_Ch = "1"$ indicating that ART has reached to the optimal resonance capacitance at that point. In Fig. 10(b), we have intentionally detuned the L_4C_4 -tank by adding external capacitors in parallel and measuring V_{REC} at steady state. It can be seen that the PMIC fails to provide the 3.3 V supply voltage with > 20 pF detuning if the ART was disabled. The ART loop, on the other hand, can maintain V_{REC} constant at 4 V for > 100 pF detuning. Table II summarizes the specification of the PMIC chip. The measured power conversion efficiency (PCE) of the rectifier versus V_{REC} for $R_L = 500 \Omega$ at $f_p = 13.56$ MHz was 76.2% when $V_{DD} = 3.3$ V and the nominal $V_{REC} = 4$ V.

Fig. 11 shows the measured transient waveforms for the current triple-loop prototype in Fig. 9 and control algorithm in Fig. 3. In Fig. 11(a), the Rx coils were suddenly moved from $d_{23} = 2.1$ cm to 2.9 cm and back to 2.0 cm away from the Tx coil. d_{23} , which was extracted from the recorded video during coil movements, is shown on the top of Fig. 11(a). It can be seen that the power control loop responds to the Rx movements within ~ 50 ms by decreasing V_{DD_PA} [1st trace on the 2nd panel in Fig. 11(a)] when d_{23} drops because V_{REC} (3rd trace) is increased above $V_{RUT} = 4.2$ V. Similarly, V_{DD_PA} increases when Rx returns to its original location and V_{REC} drops below $V_{RLT} = 3.6$ V. During this test, V_{REC} information was fed back to the Tx via back telemetry every 3.3 ms, as shown in the 4th trace on the 2nd panel in Fig. 11(a). Overall, the power loop successfully opposed to the coils' coupling variations and maintained V_{REC} and V_{DD} within their designated range. Also note that when d_{23} suddenly drops in Fig. 11(a), the OVP circuit kicks in for a brief period to protect the PMIC input from the large voltage transient across L_4 .

During the power loop operation, the Rx ART was enabled every 0.33 s for ~ 4 ms to find the Rx resonant capacitor, as shown in the zoomed inset at the bottom of Fig. 11(a). In this measurement, as expected, V_{REC} was increased when the ART was enabled because of the optimal tuning.

Fig. 11(b) shows the transient response when a 10 pF capacitor was added to L_2 in parallel at the time indicated by a vertical dashed line. V_{REC} has dropped as a result, and the

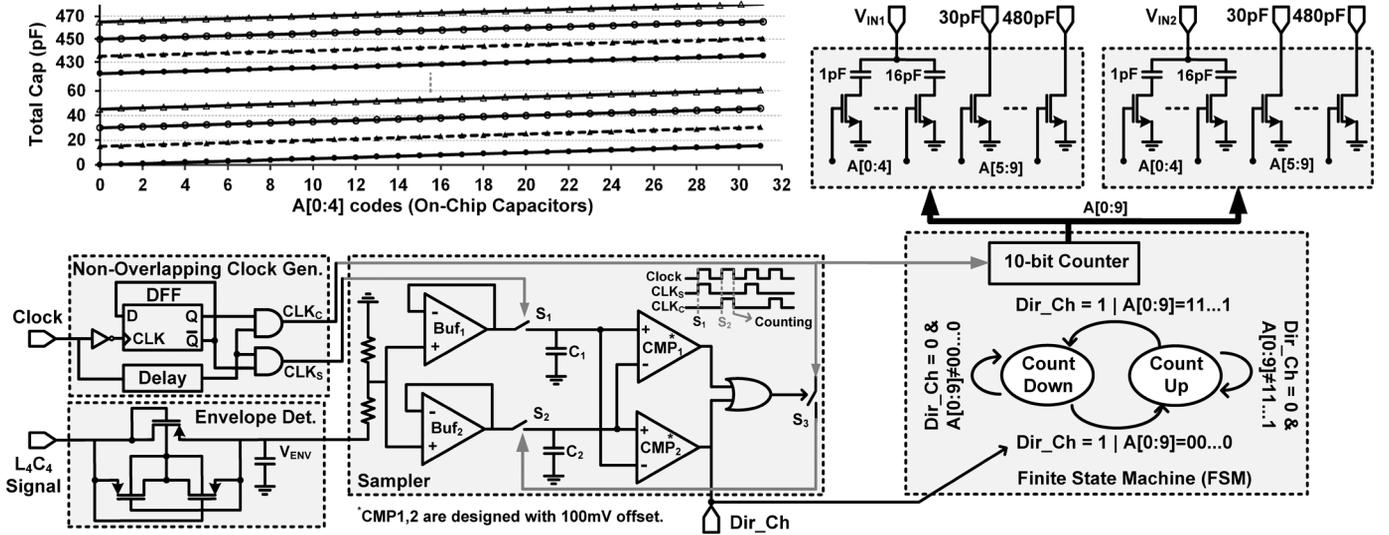
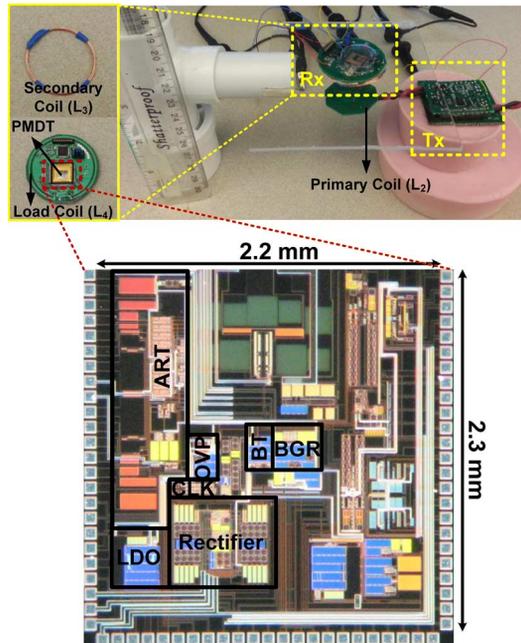


Fig. 8. Schematic diagram for the automatic resonance tuning (ART) circuit blocks in the PMIC ASIC.


 Fig. 9. Triple-loop wireless power transmission measurement setup and die micrograph of the PMIC chip, occupying $2.2 \times 2.3 \text{ mm}^2$ silicon area.

power loop has immediately taken action against this disturbance by increasing V_{DD_PA} . Once V_{REC} was returned within the desired window, the TRC loop was activated to compensate for this Tx parasitic capacitance change by elevating V_{VAR} to lower C_{Tx} . Similar to Fig. 11(a), the ART loop was also periodically enabled to find the optimal resonance capacitance for the L_4C_4 -tank. Since the ART had already found the optimal resonance condition in the earlier periods (no disturbance on the Rx side), V_{REC} was not changed significantly by the ART operation. Thanks to the TRC loop, V_{DD_PA} returned back to its original value ($\sim 3.5 \text{ V}$) before adding the parasitic capacitance, because L_2 was re-tuned at 13.56 MHz and the same amount of power was being delivered to the Rx with the same V_{DD_PA} . The transient response in Fig. 11(c) shows how V_{REC} and V_{DD}

 TABLE I
THREE-COIL INDUCTIVE LINK SPECIFICATIONS

Parameters	Measured Value
Printed-spiral primary coil (L_2)	Inductance = 361 nH
	Outer diameter = 2.8 cm
	Line width = 10 mm
	Number of turns = 4 $Q_2 = 86.1$
Wire-wound secondary coil (L_3)	Inductance = 729 nH
	Outer diameter = 3.4 cm
	Wire diameter = 0.64 mm
	Number of turns = 3 $Q_3 = 181.0$
Printed-spiral load coil (L_4)	Inductance = 607 nH
	Outer diameter = 3.4 cm
	Line width = 1 mm
	Number of turns = 3 $Q_4 = 50.1$
L_2 - L_3 nominal distance	20 mm
L_3 - L_4 separation	3 mm
Coupling coefficients	$k_{23} = 0.081, k_{24} = 0.049, k_{34} = 0.459$
Nominal load (R_L)	500 Ω
Operation frequency	13.56 MHz

drop by a sudden increase in the Rx loading from 21.7 mW to 33.9 mW. V_{DD_PA} is immediately increased by the power control loop to compensate for the higher power demand. Once the load current returns back to 21.7 mW, the OVP circuit kicks in to protect the PMIC ASIC when $V_{REC} > 4.8 \text{ V}$, similar to Fig. 11(a), while all voltages return back to their original values.

Fig. 12 compares the measured PTE, which is defined as the overall efficiency from the power supply in Tx to the load in Rx, versus d_{23} from 1 cm to 3 cm in the open-loop, power control loop only, power and ART dual-loops, and the triple-loop conditions when the environmental effects were emulated by detuning the Tx and Rx coils with 8.3 pF and 14.4 pF capacitors, respectively. In the mono-, dual-, and triple-loop measurements, we have included the power dissipation of all the additional circuits in the overall PTE. Because open-loop system should operate at the worse-case conditions to remain operational, i.e., $d_{23} = 3 \text{ cm}$ and $V_{DD_PA} = 5.5 \text{ V}$, the open-loop PTE remains

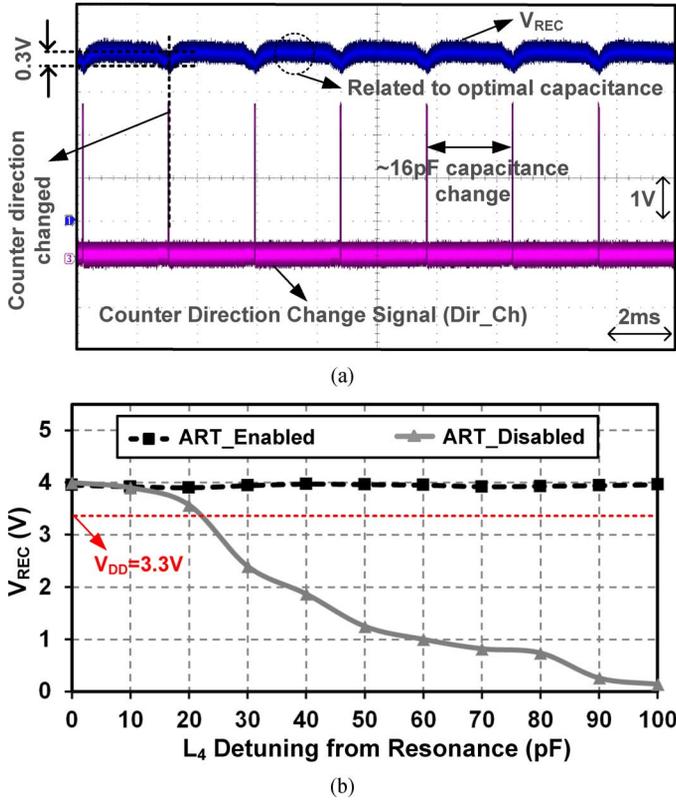


Fig. 10. Measurement results for the ART block. (a) V_{REC} and counter direction change flag (Dir_Ch) at steady state showing peaks and valleys of V_{REC} around L_4C_4 -tank resonance at 13.56 MHz. (b) V_{REC} values with and without the ART when L_4 was intentionally detuned by adding an external parallel capacitance.

TABLE II
SPECIFICATION OF PMIC ASIC

General Specifications	
Fabrication technology	TSMC 0.35- μ m 4M2P Std. CMOS
Die size (mm) / active area (mm ²)	2.3 \times 2.2 / 2.54
Supply voltage, V_{DD} (V)	3.3
Total current consumption (μ A)	68
Full-Wave Active Rectifier	
Rectifier efficiency (%)	76.2
Nominal output, V_{REC} (V)	4
Nominal loading, R_L (k Ω)	0.5
Operating frequency (MHz)	13.56
Auto-Resonance Tuning	
Operating frequency (kHz)	26.4
Tuning capacitance range (pF)	On-chip : 0-16 (5-bits) Off-chip : 15-480 (5-bits)
Back Telemetry	
Back telemetry data rate (kbps)	250
Back telemetry pulse width (ns)	\sim 250

low at shorter coil distances. However, the power loop dynamically reduces the Tx power at short distances to the level that is just enough to operate the Rx circuitry, thus significantly improving the PTE from 3% to 9.8% (6.8% improvement) at the nominal distance of $d_{23} = 2$ cm, as shown by a vertical dashed line in Fig. 12.

The PTE improvements due to the proposed ART and TRC loops highly depend on the amount of detuning in the Tx and Rx LC-tanks due to environmental effects or deformations. In our exemplar test setup of Fig. 9, when 8.3 pF and 14.4 pF detuning

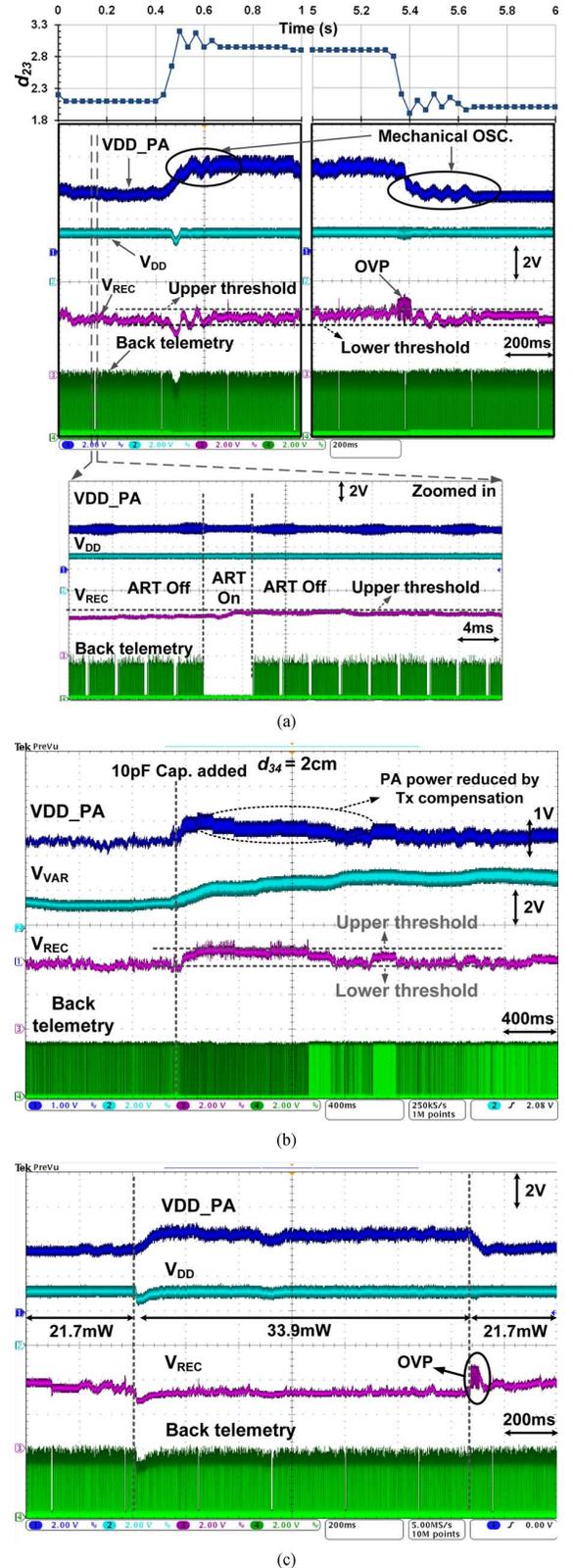


Fig. 11. Triple-loop power transmission system measured waveforms. (a) Disturbed by 0.9 cm coil distance. (b) Adding 10 pF capacitive disturbance. (c) Transient load variation from 21.7 mW to 33.9 mW.

capacitors were added to the Tx and Rx tank circuits, respectively, the PTE was improved for an additional 1.4% and 2.3% compared to the power-loop alone in Fig. 12 when the TRC and

TABLE III
BENCHMARKING OF WIRELESS POWER TRANSMISSION SYSTEM

Publication	2008 [32]	2009 [30]	2005 [35]	2009 [33]	2011 [34]	2010 [36]	2012 [38]	2013 [31]	This work
Power carrier frequency*	75 kHz	915 MHz	1 MHz	1 MHz	7.65 MHz	13.56 MHz	6.47 MHz	13.8 MHz	13.56 MHz
Coil configuration	2 coil	2 coil	2 coil	2 coil	4 coil	2 coil	2 coil	2 coil	3 coil
Closed-loop control	No	No	Yes	No	No	Yes	Yes	Yes	Yes
Adaptive Rx Tuning (ART)	No	Yes	No	No	No	No	No	Yes	Yes
Transmitter Resonance Compensation (TRC)	Adaptive carrier frequency	Yes	No	No	Yes	Yes	No	Yes	No
	Adaptive matching circuit	No	Yes	No	No	No	No	No	Yes
Tx/Rx data communication	Far field	N/A	LSK	N/A	N/A	LSK	Far field	LSK/Optical	LSK
Power Transfer Efficiency @ Distance	80% @ 1 mm	0.056%** @ 17 mm	36.3% @ 15 mm	~18% @ 50 mm	50% @ 0.7 m	6.9% @ 10 mm	75% @ 0.6 m	N/A	13.5% @ 20 mm
Tx coil diameter	N/A	20 mm	40 mm	100 mm	59 cm	20 mm	39 cm	N/A	28 mm
Rx coil diameter	N/A	2 mm	32 mm	100 mm	59 cm	10 mm	39 cm	N/A	34 mm
Potential application	IMD	IMD	IMD	N/A	N/A	IMD	Electronic appliances	IMD	IMD

* Center frequency of the tuning range

** Calculated value

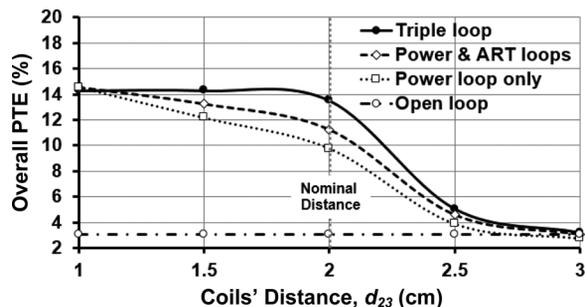


FIG. 12. Measured overall PTE versus the coil's distance in the open-loop, power control loop only, power and ART dual-loop, and the triple-loop conditions when environmental effects were emulated by detuning the Tx and Rx coils with 8.3 pF and 14.4 pF capacitors, respectively.

ART loops were activated, respectively. Table III compares this work with the most recent open- and closed-loop WPT systems in the literature in terms of the techniques used to improve the PTE. One should consider that the absolute value of the PTE is dependent on multiple parameters related to the design and application of an inductive link. Therefore, the goal was not to demonstrate the highest possible PTE, but to stabilize it by adding to the robustness of the WPT system. To the best of our knowledge, this work is the first to demonstrate the dynamic operation of all three loops along with a simple but stable control strategy in a prototype system.

VI. CONCLUSIONS

A standalone triple-loop wireless power transmission system has been demonstrated for dynamic applications in variable environments, such as implantable biomedical devices. The proposed system includes three loops to adaptively tune Tx and Rx LC-tanks to the power carrier frequency and also adjust the transmitted power in the presence of coils' coupling variations. A sequential control algorithm has been devised to activate these three loops, one at a time, while maintaining the stability of the entire power transmission link. The system dynamically maximizes the PTE of the inductive link in the presence of

various disturbances from inside (e.g., sudden loading variation) and outside (e.g., body movements, changes in the surrounding tissue morphology, flexible coil deformations, and nearby large conductive objects) the system in real-time. The prototype Tx is built around a COTS RFID with custom circuitry for the TRC. The Rx was built around a custom-designed PMIC that includes a high efficiency active rectifier, a regulator, a back telemetry circuit, and the ART. To further increase the PTE, a 3-coil inductive link was designed and used in measurements. Results showed that the proposed triple-loop WPT system and its control algorithm were stable in various conditions, and respond as expected to various types of disturbance, such as parasitic capacitors added to the Tx and Rx tank circuits, coupling variations due to coil displacements, and loading variations, while significantly improving the PTE.

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